# DESIGN, FABRICATION AND TEST OF A 15W GaN 10GHz HYBRID POWER AMPLIFIER

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## ABSTRACT

This paper describes a technique for designing saturated hybrid power amplifiers using discrete die devices in the microwave region, which is capable of achieving good agreement between simulated and measured results in one design pass.

## INTRODUCTION

The use of unpackaged die allows operation up to much higher frequencies compared to packaged devices, as the parasitics are much lower and easier to control. The typical construction of such a power amplifier will involve a metal carrier plate, usually fabricated from a thermal expansion matched material such as CuMo or CuW, probably in the region of 0.5 to 1mm thick. On this carrier will be mounted as a minimum the active device and input/output matching networks, either as two pieces or a single piece with a laser cut hole to accommodate the active device. Bias networks can be incorporated into the RF matching circuitry, or provided externally depending on the application. In the design to be described below, the carrier assembly did not include the bias networks, only the basic RF matching circuits. The amplifier was later successfully integrated into a complete assembly, including bias network on separate substrates.

## DESIGN METHOD

It may not be possible at the start of a design to specify the substrate materials (ie dielectric constant and thickness) as this will need to be investigated as part of the design work, as it can affect phase/amplitude balance of the signals across the individual cells of the device. Generally most designs that have been done within TriQuint used 0.125mm or 0.25mm thin film alumina, and more recently 0.25mm er=36 material. Minimising losses is also very important to overall performance, which may again affect the choice of materials, gold plating thicknesses etc.

The design technique to be described in this paper makes use of linear design models for the active device in conjunction with current and voltage probes located at the output of each cell of the device. Small signal responses are predicted using small signal models. Output power and efficiency are predicted using measured load pull data and Cripp's methodology, using equations within the simulator to calculate the power delivered by each cell of the device into its individual load impedance as determined by the current and voltage probes. The equations make use of measured load impedance data obtained from load-pull measurements, together with measured output power and drain current. This method is described in detail in Ref 1. The advantage of this method is that is seems to give more accurate predictions of saturated amplifier performance when compared to large signal device models, and also allows unbalance effects between individual device cells to be investigated and corrected by layout or bonding changes. Individual cells can thus be loaded more equally with consequences of better reliability, power output and efficiency.

The design methodology used in this application note applies equally to design using probe-based analysis or non-linear design methods.

## DESIGN EXAMPLE: 10GHz POWER AMPLIFIER USING TRIQUINT GaN DEVICE (TGF2023-05).

This design was undertaken to investigate what performance could be obtained with the TGF2023-05 GaN discrete HEMT in the 10-10.5GHz region.

The first stage in the design was to construct a model for the 4 cell device using Triquint data sheet small signal models and differential source inductance for the outer cells, following the same methodology that had been used to generate the s-parameter models published on the TriQuint website (Ref 2). The 1.25mm unit cell (UGC) is shown in Fig 1, and the complete 5mm device in Fig 2.

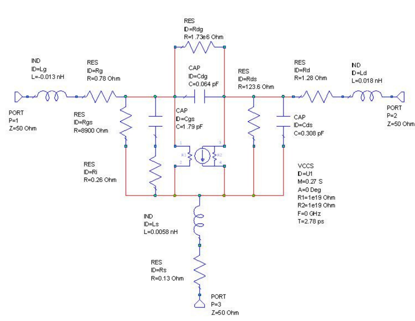



Fig 1: Schematic of 1.25mm unit cell (UGC)

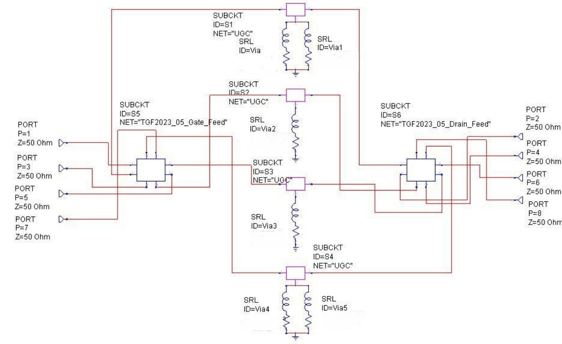



Fig.2: Schematic of complete FET

The complete device is constructed from 4 UGCs, electromagnetic (e-m) simulations of the on-chip gate and drain feed networks, and source via models. Note that the "internal cells" are connected to ground by a single via while the outer cells have slightly lower inductance to ground. This technique can be extended to larger periphery devices, where the outer cells have the extra vias. The complete FET is connected into the circuit as an 8 port block.

The amplifier was simulated using a linear circuit simulator. It was decided to use distributed matching elements for both gate and drain matching circuits, on 0.125mm thick (as fired) alumina substrates. The use of lumped element pre-matching for each cell of the device had been investigated previously, and although good results were obtained in the simulator, it proved very difficult to realise the circuits in practice owing to tolerances in component placement and wire bond lengths.

The gate and drain feed sections were set initially to be wide enough to connect to the device. A number of topologies for the remainder of the elements were investigated initially, and for the input a combination of a shunt open-circuit stub, and series transmission line prior to the device feed line provided an adequate small-signal match across the band. The output network required only an extra length of transmission line in addition to the drain feed line. Constrained optimization was then used to find optimum lengths and widths for the transmission lines. Gate and drain bondwire inductances were modeled at this stage as equal value uncoupled pure inductors, which were included in the optimization process (separately for gate and drain). A schematic of the amplifier after optimization is shown in Fig 3.

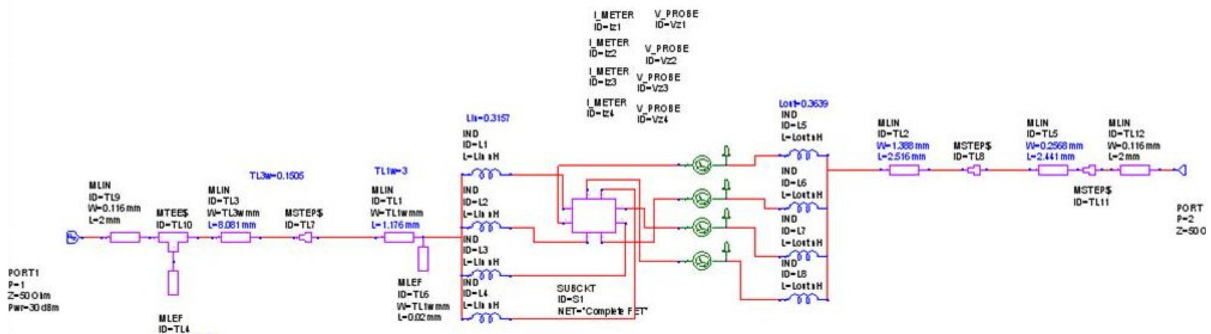



Fig 3: Schematic of basic amplifier

The next stage in the design was the replacement of the simulator's model of the transmission lines feeding the gate by an e-m simulation of the layout. This was done for two reasons, to model the linewidth discontinuities more accurately, and to allow the connections to the gate bonds to be made at the actual physical positions along the end of the transmission line corresponding to the gate pads on the device. The layout of the e-m simulated element is shown in Fig. 4 .

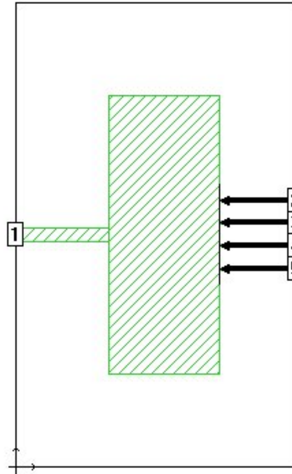
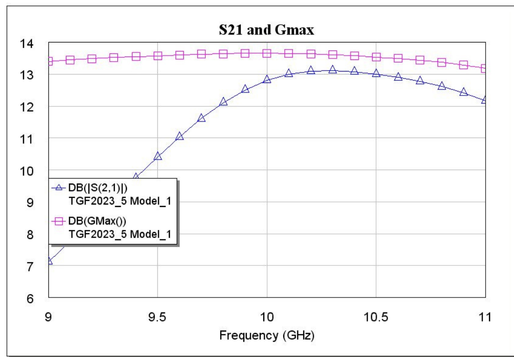



Fig 4: e-m simulation layout of last section of input matching network.

The element included a 1mm length of line of the same width used to feed wider line from the input side connected to Port 1, and 4 lines 0.025mm width connected to the other side of the wide line, connected to Ports 2-5. The reference planes for Ports 2 to 5 were set to the right hand edge of the wide line.

The s-parameters of this element were imported into the simulator and replaced the standard transmission line model for the wide section of line (the length of the line feeding it was reduced by 1mm to allow for the section included in the e-m simulation). The small signal gain response of the amplifier before and after these changes are shown in Figs. 5 and 6.



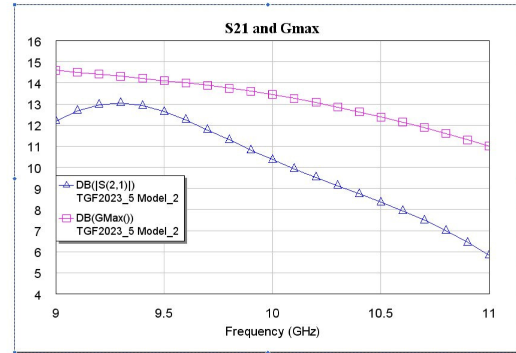




Fig 5: Predicted S21 using standard models

Fig 6: S21 after including e-m simulation

It can be seen that the effect of using e-m simulated s-parameters for the wide line feeding the gate bondwires instead of the simulator's transmission line model, and a single point of connection for the gate bondwires, was to shift the gain response approximately 1GHz lower in frequency. This shows the value of using e-m simulations for the networks instead of simple transmission line models.

The shifted frequency response was corrected by re-optimizing the dimensions of the standard open circuit stub, the following transmission line and the inductance of the gate bondwires. Next, the individual gate bondwires were replaced by the simulator's multiple bondwire model, configured for 4 wires, to provide a more accurate representation of multiple bondwires. This allows for the effect of the groundplane and mutual inductance

between wires. The length element was optimized, together with the other transmission line elements to recover the gain response. The wires were spaced to correspond with the spacing of the gate pads on the device.

As with the gate circuit, e-m simulation was performed on the first element of the output network, and the layout of this is shown in Fig. 7.

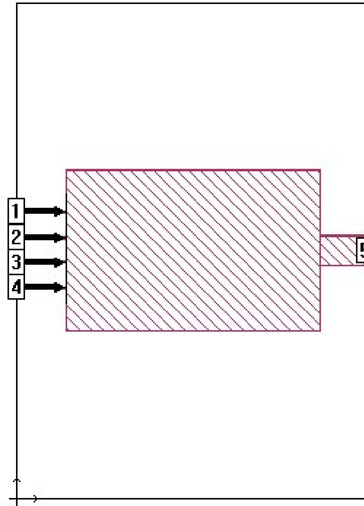



Fig 7: e-m simulation layout of first section of output matching network

Simulated output power and PAE for the simulator's model are shown in Fig. 8 and for the e-m simulated model in Fig. 9.

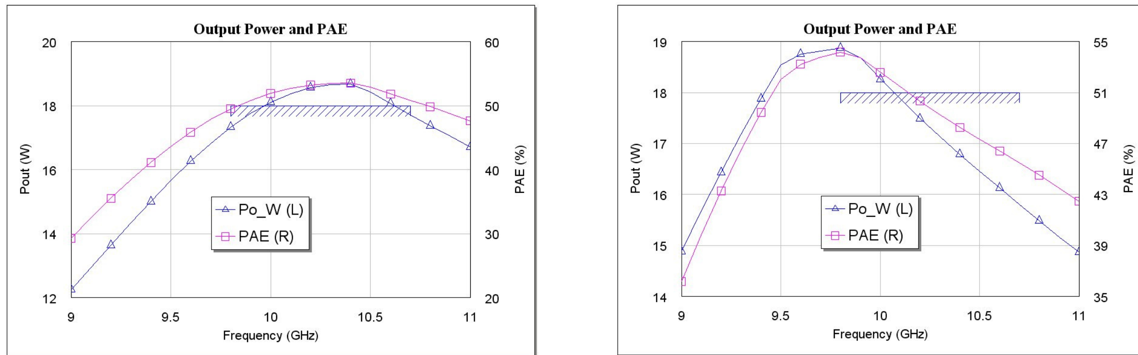



Fig. 8: Simulated Pout and PAE using standard models Fig. 9: Simulated Pout and PAE using e-m simulation

A shift in frequency response of approximately -500MHz was observed, and was corrected by re-optimizing the parameters of the models for the drain bondwires and the series transmission line following the e-m simulated line. The drain bondwires were then replaced by the multiple bondwire element, and the circuit re-optimized. The predicted output power dropped by about 700mW after adopting the BWIRES2 model for the drain

bondwires. This could be recovered by either adding extra inductance to the outer wires (about 0.05nH), or by moving the outer wires away from the inner wires by about 0.3mm. Later it was found that slightly better performance could be obtained by moving the wires at the device drain, instead of moving them where they connected to the drain matching circuit. The need for extra inductance for the outer wires is attributed to equalizing the load impedances for the outer cells of the device owing to differing inductance for the inner and outer output bondwires as a result of using the multiple bondwire model.

The final stage in the design, prior to moving to e-m simulation of the complete input and output networks was to replace the single open circuit stub in the input circuit by a symmetric pair of stubs, mainly to reduce the opportunity for field asymmetry between the four ports output ports of the input network.

After re-optimization, the complete input network was e-m simulated. The gain response of the amplifier shifted by approximately +300MHz after incorporating the e-m simulation. Minor adjustments were made to the layout using the e-m simulator's "reshape" tool until the gain response was shifted back on frequency. The complete output network was also simulated, and similar adjustments made to correct a small change in frequency response. The final schematic of the amplifier is shown in Fig. 10 and the layout in Fig. 11.

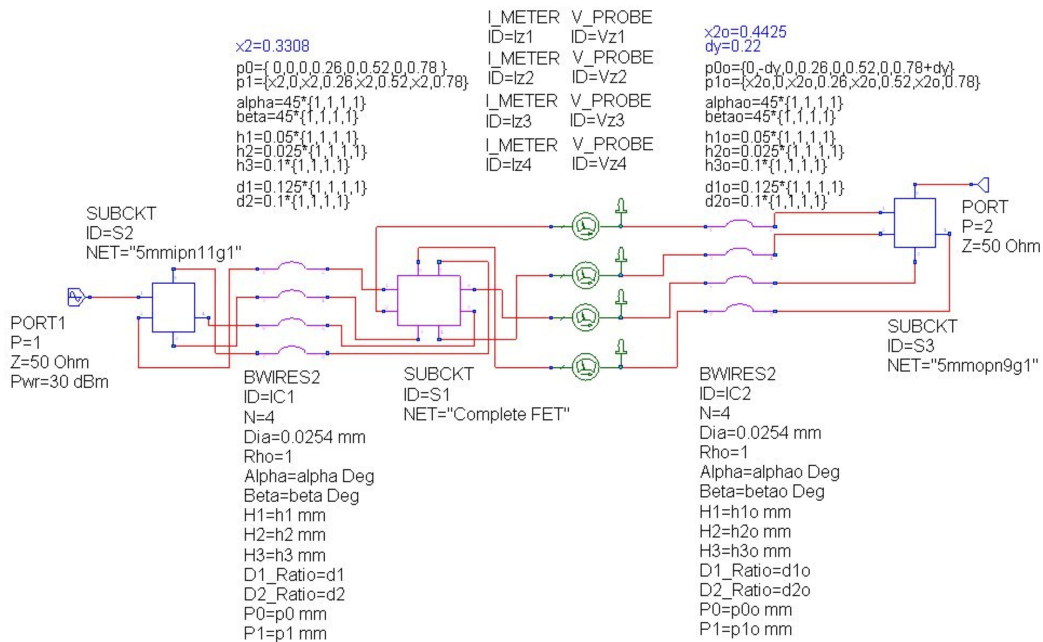



Fig 10 Schematic of final amplifier design

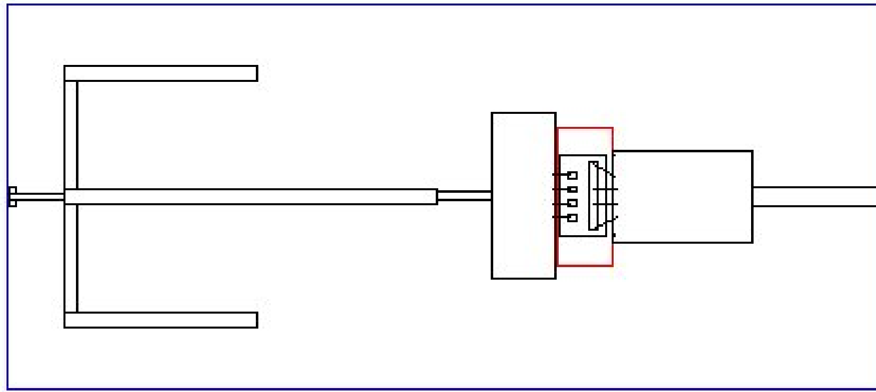


Fig. 11: Layout of final amplifier design

MEASURED RESULTS

The amplifier was constructed on a 0.5mm thick CuMo carrier and die attach used AuSn eutectic solder. A photograph of the assembly is shown in Fig 12.

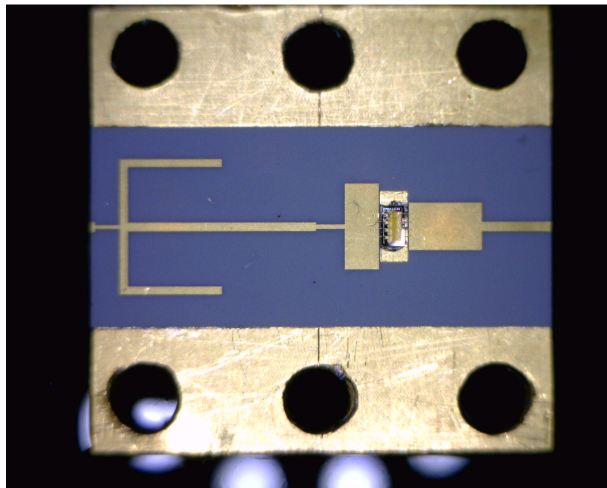


Fig 12: Photograph of amplifier carrier

Initial testing was carried out using external custom bias tees, fabricated on 0.5mm thick er=3.38 material. Gate and drain DC blocking was accomplished using 1pF low loss 0603 chip capacitors. Gate bias feed was via a 22 ohm resistor decoupled by a 0.47uF capacitor. Drain decoupling was provided by a 1uF capacitor.

Measured and predicted small signal responses of the amplifier are shown in Figs 13 to 15.
In these figures, the simulation file was edited to reflect actual wire bond lengths and location after assembly, so that the comparison reflects the amplifier as-built.

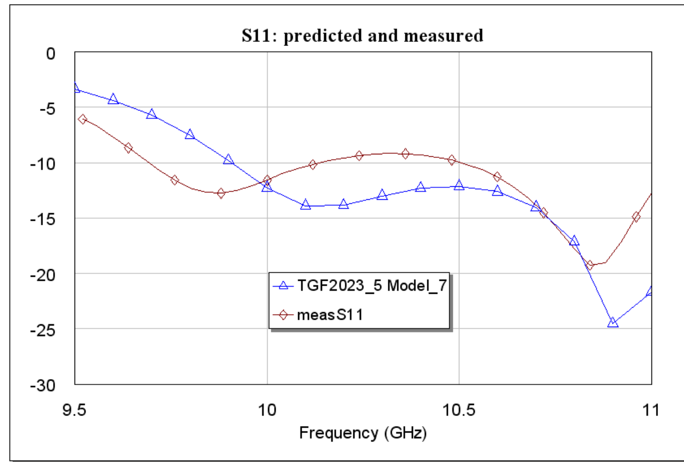



Fig 13: Input return loss

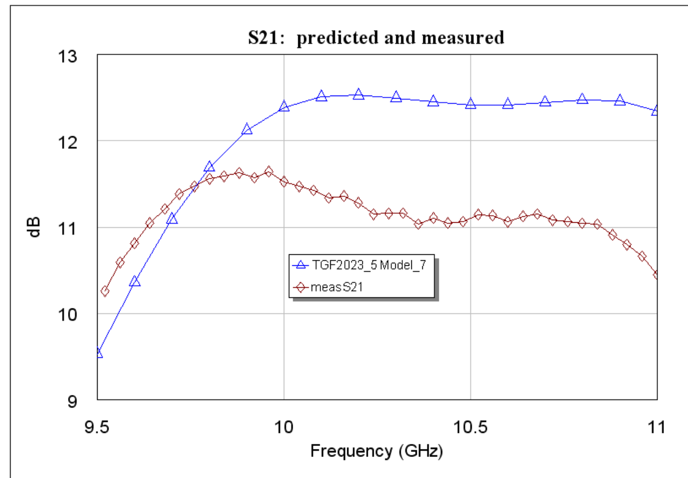



Fig 14: Small Signal Gain

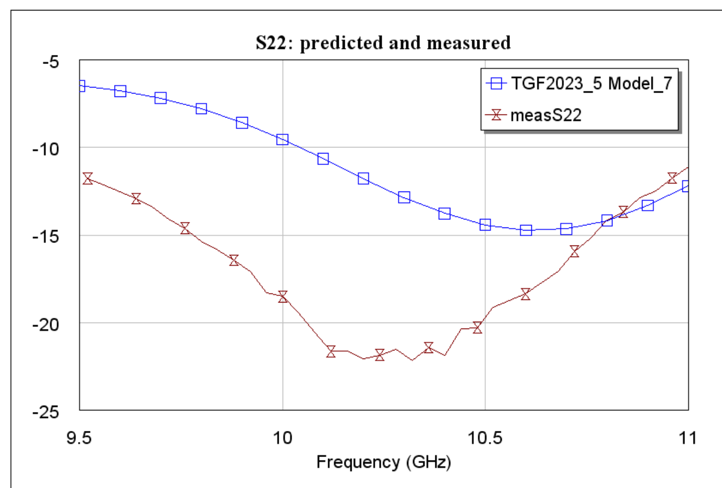



Fig 15: Output return loss

CW power output and power added efficiency measurements were made across frequency, with the amplifier driven to approximately 2dB into compression, and the results are shown in Figs 16 and 17.

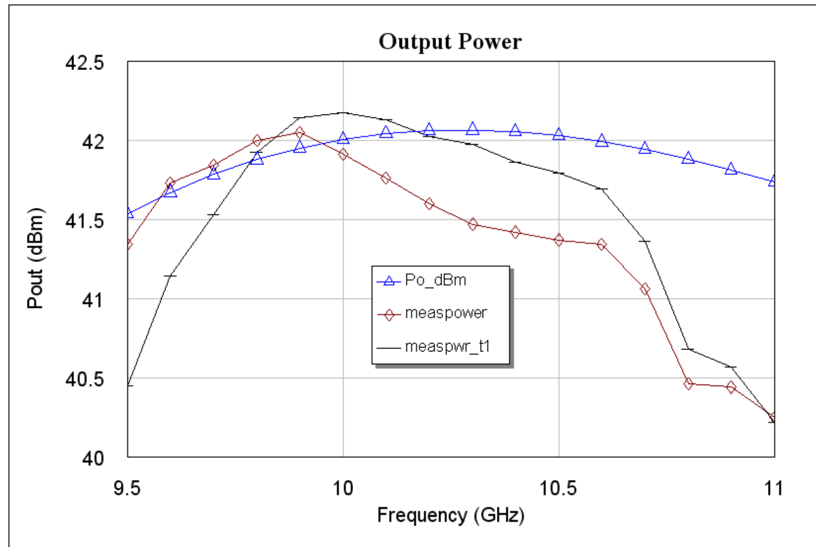



Fig 16 Output Power

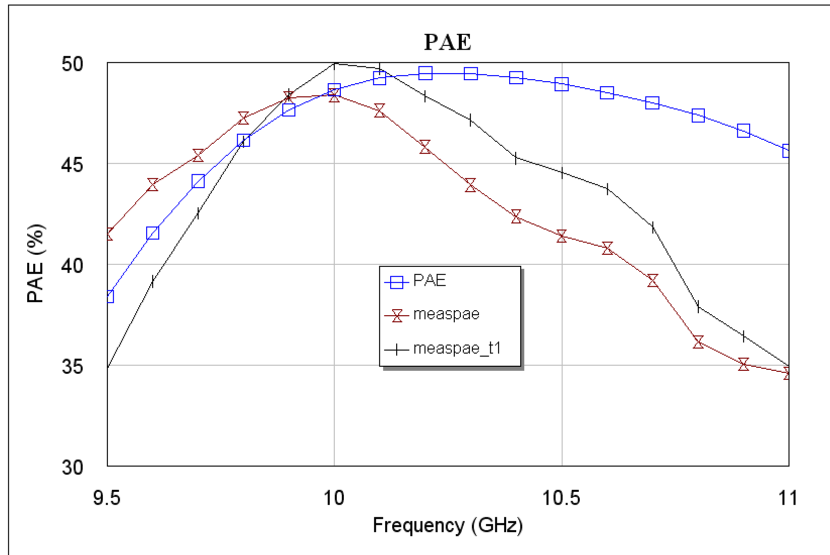



Fig 17 Power Added Efficiency

These figures also show results obtained after some additional tuning had been added to improve performance (gold foil mounted with conductive epoxy) (traces labelled. "t1"). The tuning elements are shown in Fig 18.

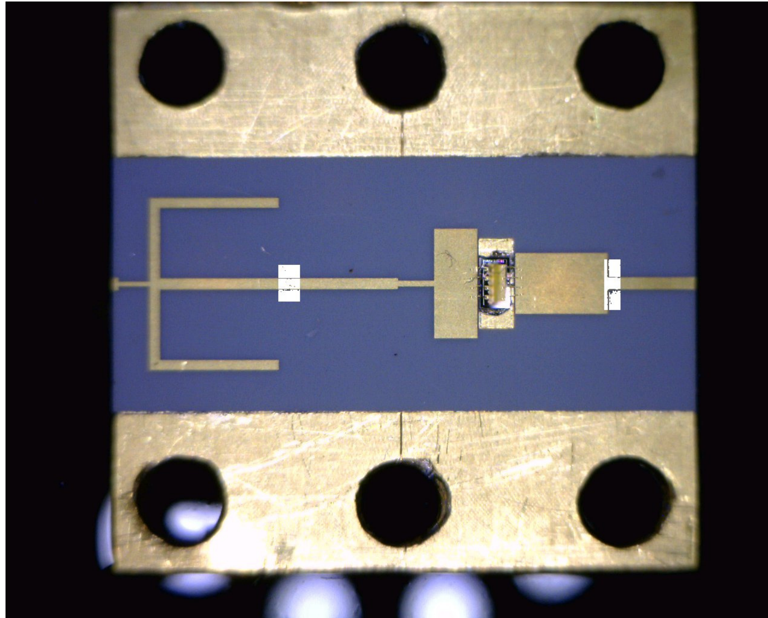


Fig 18: Amplifier after tuning

A complete amplifier was constructed using the carrier described above and bias tees. A photograph of this is shown in Fig 19. The performance of this amplifier was close to that of the carrier alone.

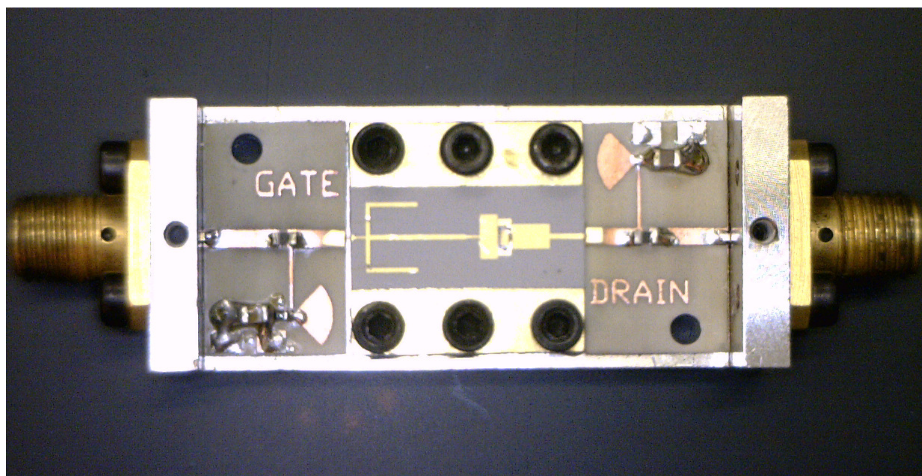



Fig 19 Carrier and bias feeds integrated into one assembly

DISCUSSION

It can be seen from the measured results that both small and large signal responses for the first pass design agree quite well with the simulated responses. The measured small signal gain is approximately 1.5dB lower than simulation, and this is thought to be due to the higher channel temperature of the 4 cell transistor compared to the single 1.25mm cell which was characterized to generate the small signal model. Other results , not presented here, have shown better agreement in pulsed applications, where the channel temperature is considerably lower than in the present (cw) application. The thermal design of the amplifier has been improved since the data shown above was taken, and more amplifiers are awaiting evaluation. These incorporate different schemes for improving the heat transfer from the carrier to the baseplate.

The measured output power was within about 0.5dB of simulation for the as-built amplifier across the band of interest. Measured PAE was about 5 points lower on average, which is largely attributed to the lower gain.

Both output power and PAE were capable of improvement by adding some small extra tuning elements to the circuit. This is quite common with this type of amplifier realization, where is it not generally possible to get exact agreement between simulation and measurement. The location and size of these tuning elements were consistent over several amplifiers, so could be easily incorporated into a second design pass.

The value of using electromagnetic simulation for the matching networks has been demonstrated. If simple transmission line models had been used instead, the measured amplifier responses would have been shifted in frequency by approximately 1GHz., and it would probably not have been possible to recover performance by tuning. Also, the matching topology used was chosen to be suitable for accurate simulation and practical realization. . Other topologies had been tried in the past using lumped components (bondwire inductors and discrete capacitors). These were found not only to be difficult to simulate, but also very difficult to fabricate with the required precision, leading to disappointing amplifier performance.

Ref 1: C. Campbell, “Probe Based Simulation Technique for Modeling Saturated Power Amplifiers”, European Microwave Conference 2011

Ref 2: http://www.triquint.com/prodserv/more_info/proddisp.aspx?prod_id=TGF2023-05