

Key Performance Parameters of ESD Protection Devices for High Speed I/O, RF and Monolithic Microwave Integrated Circuits

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Abstract—Damage by electrostatic discharge (ESD) is a permanent threat to valuable electronics. Data and audio ports, antennas, keypad, touchscreen as well as displays are exposed to dangerous transients origin from electrostatic discharge either triggered by contact to human beings or any objects carrying electrostatic charge. A well established solution to protect circuitry from these destructive ESD events is to shunt most of the ESD pulse energy by transient voltage suppressor (TVS) diodes thereby reducing the residual transferred energy to the protected device to a minimum. However, using advanced semiconductor technologies the ESD susceptibility of ICs are subsequently getting higher. By the same time, data rates of I/O ports are increasing, reaching far into the GHz regime. A challenge for the protection device design is to balance both, superior protection characteristics as well as minimum impact to the nominal function of the circuitry, i.e. maintaining highest signal integrity.

In this paper ESD is investigated as a specific, but well determined operating condition of integrated microelectronics, characterized by fast transients and high power, thus requiring specific measurement techniques ...

I. INTRODUCTION

Electro Static Discharge (ESD) is the rapid and uncontrolled transfer of electrostatic charge between bodies with different electrostatic potentials. ESD is a single event with high currents up to $30 A_{Peak}$, high voltages up to $30 kV_{Peak}$ and very fast transients in the range of 1 ns to 300 ns.

ESD is a high cost factor for the industry as it is one root cause of device, product and sytem failures. The industry has developed standards to describe and test for ESD susceptibility, the Charged Device Model (CDM), Machine Model (MM) and the Human Body Model (HBM). The CDM describes the accumulation of static charge on a device in a production environment where the device is frequently moved across working surfaces or gets contact with packaging materials. The MM is similar to the CDM and takes account for the discharge between manufacturing equipment. Both standards, MM and CDM, refer to ESD in well controlled environments.

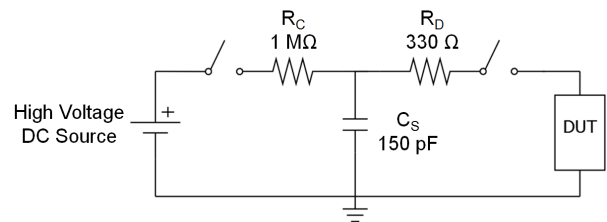


Fig. 1. IEC 61000-4-2 Test Circuit

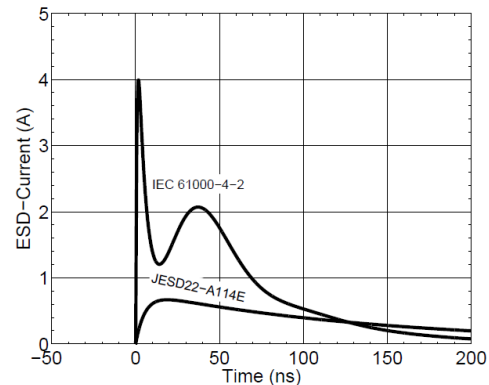


Fig. 2. Comparison of a 1 kV component-level ESD pulse according HBM JS-001-2012 ($R=1.5 k\Omega$, $C=100 pF$) and a 1 kV system-level ESD pulse according IEC 61000-4-2 ($R=330 \Omega$, $C=150 pF$)

A. Human Body Model

Human contact or air discharge is described in the HBM [1]. One type of HBM ESD standard according to JS-001-2012 determines the necessary arrangements for handling integrated circuits and is often referenced as component level ESD. The ESD stress levels range from 500 V to 4 kV and are applied with a test circuit consisting of a 100 pF storage capacitor and a 1.5 k Ω discharging resistor. Another HBM ESD standard is IEC 61000-4-2 [5] which was introduced to determine the susceptibility of products and systems to human body ESD. It differs significantly from the JESD22-A114E HBM standard. The IEC 61000-4-2 test circuit

has a 150 pF storage capacitor and a 330 Ω discharging resistor, Figure 1, and tries to attempt real world ESD events. The initial peak pulse current of the ESD transient can reach up to 30 A. Figure 2 shows a comparison between HBM JS-001-2012 and HBM IEC 61000-4-2.

B. Transmission Line Pulse (TLP)

TLP generates a rectangular voltage waveform with 50 Ω source resistance. IEC 61000-4-2 generates a different waveform shown in Figure 2 at different time variant source impedance. The big advantage of TLP is the well defined and exact controllability of the waveform parameters such as source impedance, pulse width, risetime and amplitude [1]. By calculating the pulse energy of a IEC 61000-4-2 waveform a correlation factor of $2 A_{TLP} \text{ Pulse Current} / kV_{IEC 61000-4-2} \text{ Pulse Voltage}$ can be found. The TLP technique enables the designer to find, analyse and improve the ESD protection concept for a system [2].

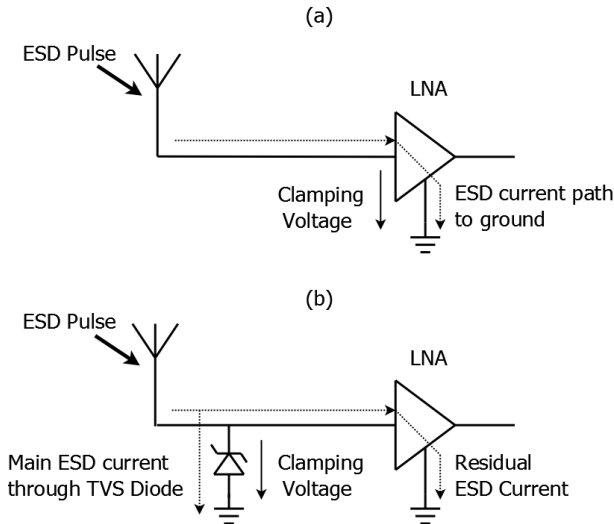


Fig. 3. LNA application circuit without ESD protection (a) and with ESD protection (b)

1) *TLP Analysis Example:* Figure 3a shows a circuit with a low noise amplifier (LNA) and an antenna. In case of ESD at the antenna the LNA input will dissipate all the energy of the ESD pulse. The measured TLP I/V characteristic of the LNA input with and without external ESD protection is shown in Figure 4. On the x-axis of the graph the measured clamping voltage at the DUT is applied, the y-axis shows the TLP current flowing into the DUT. It can be seen from the TLP I/V curve, point (V_{t2}, I_{t2}) , that the LNA fails at 3 A TLP current with a measured clamping voltage of 5.4 V at the LNA input. The second curve shows the same measurement with a transient voltage suppressor (TVS) diode in shunt configuration placed in front of the LNA input, Figure 3b. When the TVS diode turns on, point (V_{t1}, I_{t1}) , a low impedance path is formed and shunts most of the ESD current to ground. The

LNA can now withstand 12 A TLP current, before the LNA input reaches the 2nd breakdown, point (V_{t3}, I_{t3}) , Figure 4. At point (V_{t3}, I_{t3}) the TVS diode's clamping voltage exceeds the maximum clamping voltage level allowed at the LNA input. The maximum ESD current the LNA can withstand in the application circuit is now determined by the clamping voltage of the TVS diode. The clamping voltage of a TVS diode can be calculated from datasheet values, dynamic resistance and breakdown (trigger) voltage, Eqn. 1, or read out from the TVS diode's TLP I/V curve.

$$V_{Clamp} = R_{Dyn} \cdot I_{TLP} + V_{Breakdown} \quad (1)$$

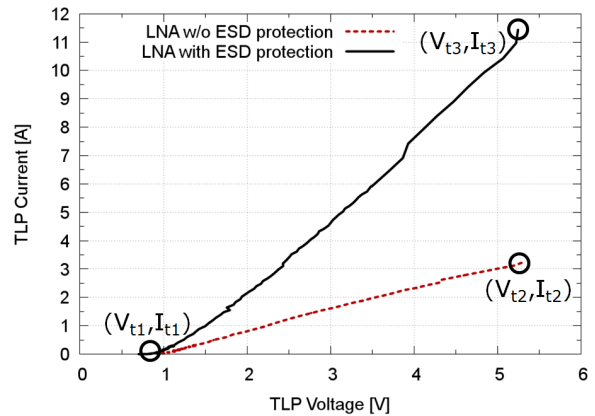


Fig. 4. TLP I/V Curve of a Low Noise Amplifier with and without external TVS Diode

II. ESD PROTECTION DEVICE KEY PARAMETERS

ESD protection devices shunt most of the ESD pulse energy to ground and thereby reducing the residual transferred energy to the protected device to a minimum. Besides the protection capability the ESD device must not influence the proper functionality of the protected system. Therefore a fair trade-off between ESD capability and signal integrity must be made. Following key parameters which influence ESD capability and signal integrity have to be considered:

- Dynamic Resistance
- Clamping Voltage
- Diode Capacitance
- Insertion Loss
- Harmonic Distortion
- Intermodulation Distortion
- Leakage Current
- Breakdown Voltage

A. Dynamic Resistance

Dynamic resistance determines the clamping voltage of the TVS diode and the dissipated energy into the protected circuit. Both, dynamic resistance and clamping voltage describe the TVS diode's internal behaviour when operated in the high current domain for a short period of time, e.g. in case of an ESD

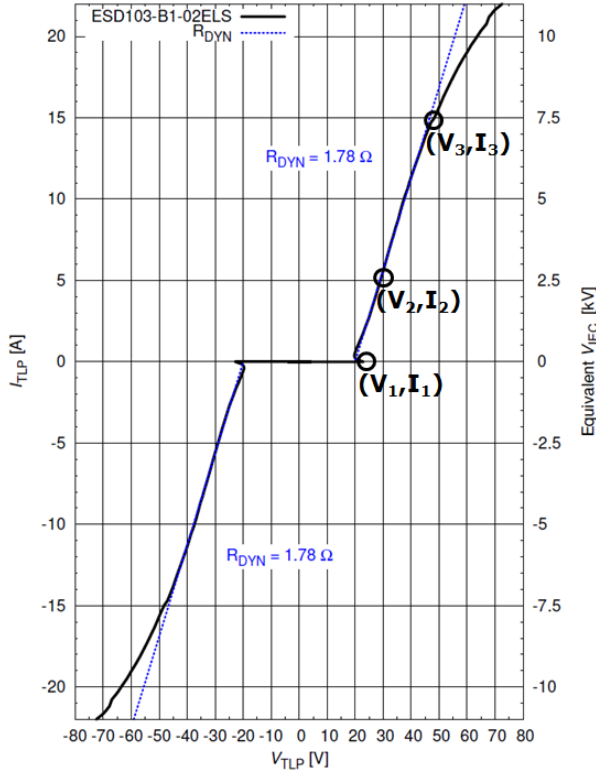


Fig. 5. TLP I/V curve of a bidirectional 100 fF TVS diode

event. TLP I/V characteristics of a sub 100 fF bi-directional TVS diode are shown in Figure 5. The dynamic resistance can be extracted from the TLP I/V plot with two points, Eqn. 2:

$$R_{dyn} = \frac{V_3 - V_2}{I_3 - I_2} \quad (2)$$

As can be seen in Figure 5 the diode triggers at 22 V, point (V_1, I_1) and snaps back to 20 V. This snapback further reduces the clamping voltage and respectively the energy dissipated in the protected device. For example the energy dissipated into a 50Ω load of an unclamped 8 kV IEC 61000-4-2 pulse would be reduced by 28 dB from 682000 nWs down to 922 nWs. Figure 6 shows a 8 kV IEC 61000-4-2 clamping voltage curve of a bi-directional 100 fF TVS diode measured into a 50Ω load with a 6 GHz sampling oscilloscope at a sampling rate of 20 GS/s, see Figure 7 the corresponding measurement setup.

B. Capacitance

Silicon diodes in general have non linearities. The voltage and frequency dependent capacitance, non linear forward I/V behaviour as well as conductivity modulation in the base region of P-I-N diodes. Figure 8 shows the junction capacitance versus reverse working voltage of a sub 100 fF TVS diode measured at 1 MHz and 1 GHz.

For small signal amplitudes a packaged diode can be represented as a series resonant circuit consisting

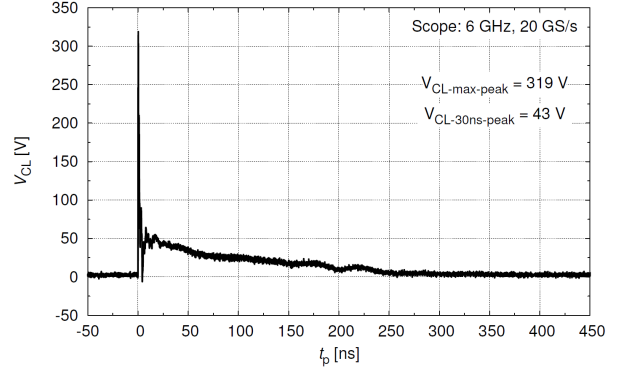


Fig. 6. 8 kV IEC 61000-4-2 Clamping voltage of a bi-directional 100 fF TVS diode

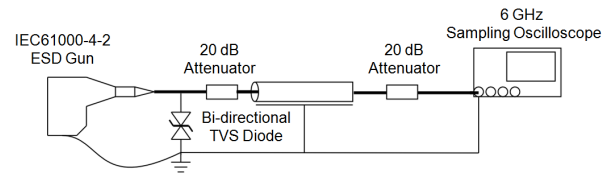


Fig. 7. IEC 61000-4-2 Clamping voltage Measurement Setup

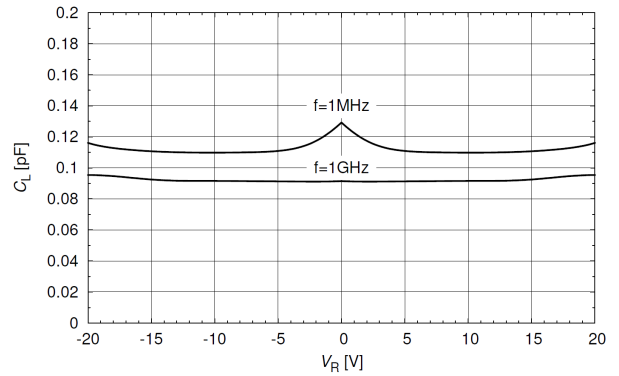


Fig. 8. TVS Diode Capacitance versus reverse voltage

of the junction capacitance C_j and the bond wire inductance L_b , Figure 9. Since the capacitance of

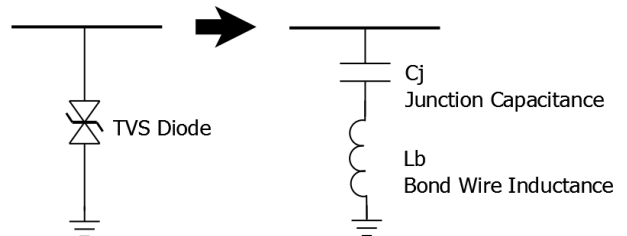


Fig. 9. Simplified small signal equivalent circuit of a TVS diode

the example diode is less than 100 fF and the bond wire inductance 0.2 nH the resonance frequency and 3 dB bandwidth is far beyond 20 GHz. Small signal insertion loss, a key characteristic for RF applications and mainly determined by the junction capacitance and bond wire inductance [3], is less than 0.4 dB at 20 GHz, Figure 10.

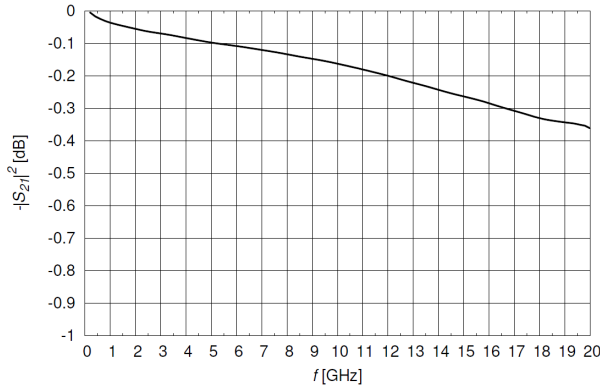


Fig. 10. Insertion Loss of a bi-directional sub 100 fF TVS diode

Harmonic distortion and intermodulation distortion products are generated by the diode's non linearities. Especially in large signal, high power RF applications harmonic generation can be a major concern. Besides other non linearities, the capacitance versus voltage, dC/dV , characteristic contributes significantly to the non linear effects, Figure 8. Figure 11 and Figure 12 show the harmonic generation at GSM frequencies for power levels up to 36 dBm.

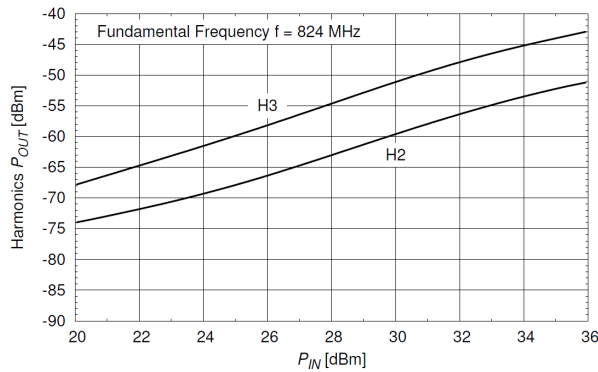


Fig. 11. Harmonic generation at GSM low band frequency $f_C = 824$ MHz

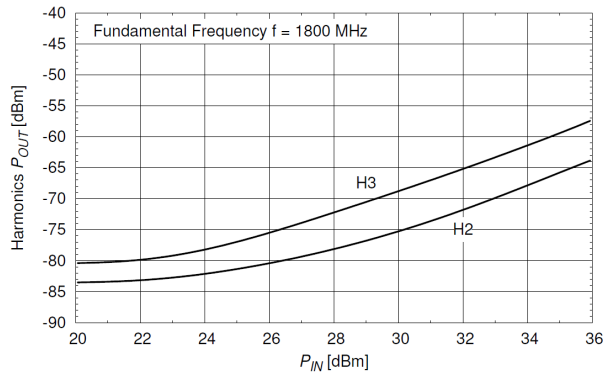


Fig. 12. Harmonic generation at GSM high band frequency $f_C = 1800$ MHz

2^{nd} harmonic power is below -50 dBm and 3^{rd}

harmonic power below -40 dBm. Due to the decreasing dC/dV behaviour with increasing frequency harmonic products at higher fundamental frequencies are decreased. A bi-directional TVS diode is suppressing the even order harmonics (2^{nd} , 4^{th} , ...) due to its balanced configuration [3], Figure 13.

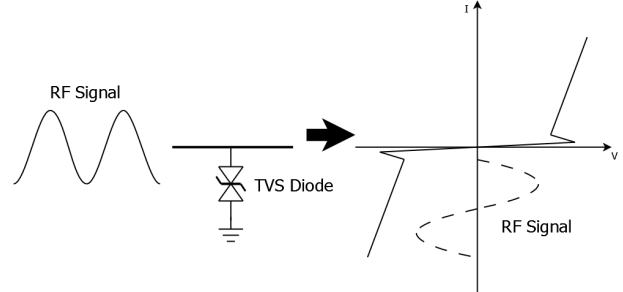


Fig. 13. Balanced configuration of bi-directional TVS diode

In high power RF applications the mixing of one signal with an unwanted intermodulator can cause in band distortion products. A common measure for this is intermodulation distortion [4]. For Example the mixing product of the GSM band I TX signal ($f_{TX} = 1950$ MHz) with a neighbouring TX signal ($f_{Blocker} = 1760$ MHz) falls into the GSM band I Rx frequency ($f_{RX} = 2140$ MHz) according to Eqn. 3:

$$f_{RX} = 2f_{TX} - f_{Blocker} \quad (3)$$

The measured intermodulation distortion product for GSM band I, $f_{Blocker} = 1760$ MHz, is shown in Figure 14. The corresponding measurement setup can be seen

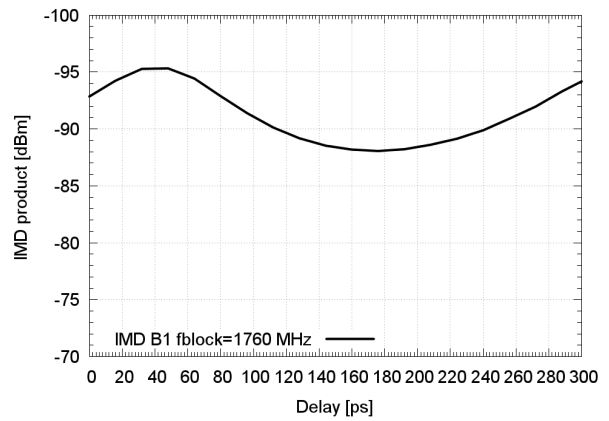


Fig. 14. Intermodulation distortion for GSM band I, $f_{Blocker} = 1760$ MHz, $P_{Blocker} = -15$ dBm, $P_{TX} = 20$ dBm

in Figure 15.

III. CONCLUSION

The influence of a ESD protection diode under high power and high frequency conditions was shown on a 100 fF Infineon ESD103 TVS diode. Contribution of the diode's dynamic resistance and capacitance to ESD protection capability and RF performance parameters,

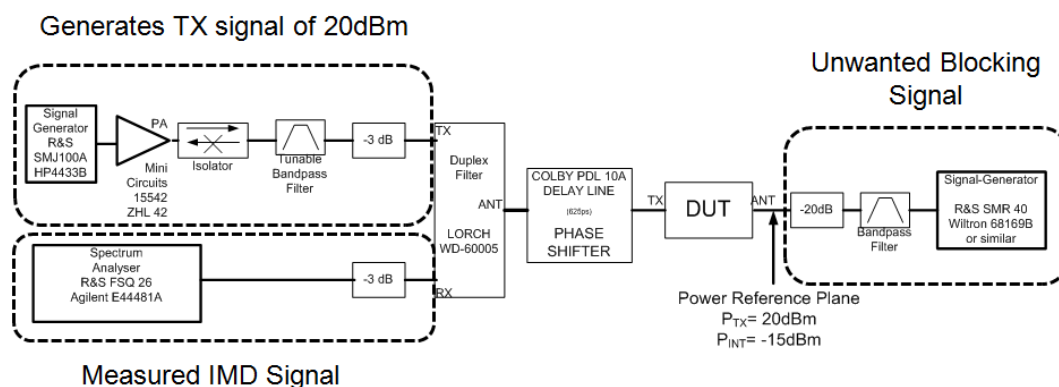


Fig. 15. Intermodulation distortion setup according to [4]

e.g. harmonic distortion, intermodulation distortion and insertion loss, was analysed by measurements. Due to its high linearity and high reverse working voltage of ± 15 V the ESD103 is very well suited for high frequency and high power applications. For high speed data applications like USB3.0 a low voltage version of the ESD103 with a reverse working voltage of 5.3 V could be used.

REFERENCES

- [1] JS-001-2012, *For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)- Component Level* JEDEC Solid State Technology Association, April 2012
- [2] Infineon Technologies: *Application Note No. 210: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology*
- [3] Infineon Technologies: *Application Note No.178: ESD Protection for RF Antennas using Infineon ESDOP4RFL and ESDOP2RF*
- [4] T. Ranta, J. Ellä and H. Pohjonen *Antenna Switch Linearity Requirements for GSM/WCDMA Mobile Phone Front-Ends*
- [5] International Electrotechnical Commission, *Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test* 9th December 2008, ISBN 2-8318-1019-7, <http://www.iec.ch/>
- [6] JESD22-A114D, *Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM)* JEDEC Solid State Technology Association, March 2006
- [7] PROTEK DEVICES, *ESD Standards vs Real-World Conditions* Technical Article, May 2011