Cost-Effective Hybrid Input-Matched GaN Transistor for S-band Radar Applications

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Introduction

The use of Gallium Nitride (GaN-on-SiC) technology in high performance RF power amplifiers (PAs) is now widespread. Whilst the cost per unit area of GaN is still higher than that of competing technologies such as Gallium Arsenide (GaAs) or LDMOS, the technology has now matured to the point where the transistor cost per Watt of RF output power is lower than GaAs. Active phased-array radars can contain hundreds of amplifiers, so any cost reduction that can be achieved on a single amplifier quickly adds up to significant cost savings. At the same time, the RF performance of the system is paramount, and power amplifiers that use GaN-on-SiC transistors have achieved excellent power and efficiency.

Plextek RFI has worked with Qorvo to design the QPD1020 hybrid input-matched GaN transistor, which includes internal input matching realised on a passive GaAs die. Unlike a pre-matched transistor, which is not fully matched to 50 Ω, the input of this transistor is internally matched to 50 Ω. This transistor is termed 'hybrid' due to its use of two separate semiconductor technologies. This approach provides the performance of GaN and the convenience of internal input matching at a reduced cost compared to a GaN MMIC.

The QPD1020 internal input matching is designed for the 2.7 – 3.5 GHz frequency range. For S-band radar applications it is common to only use part of the frequency band. The output matching network can therefore implemented on the PCB to allow large-signal performance to be optimised for output power or efficiency (or a compromise between the two) over the desired frequency band.

The QPD1020 can be used as an output stage in an active phased-array radar system or as a driver amplifier for a higher power output stage. An accompanying PA reference design with an output matching network tuned for optimum efficiency between 2.7 to 3.1 GHz has also been developed and is described below.

Hybrid Input-Matched Transistor Implementation Strategy

There are several practical approaches for the realisation of GaN power amplifiers; a comparison of these options is presented in Table 1.

GaN MMICs, internally matched to 50 Ω at both input and output, have the potential to provide the best RF performance, particularly at higher operating frequencies, and require the least space on a PCB. However, it is generally the most expensive of the options considered and cannot be optimised

for different operating bands. An example of a fully 50Ω matched single-stage GaN PA design operating at X-band is described in [1].

A PA implemented using a discrete packaged GaN transistor is often the lowest cost option, although it also tends to be the largest size. Examples of the design and realisation of a range of GaN PAs using discrete unmatched transistors, is described in [2]. In addition to occupying the most PCB space, this approach also requires the highest level of design effort by the customer.

The per-area cost of GaN-on-SiC is undeniably higher than GaAs, especially when compared to a passive GaAs process with relatively few fabrication steps. It therefore makes sense to consider the use of a low-cost passive GaAs process for the input matching network and a high-performance GaN process for the transistors. Such a composite input-matched transistor allows costs to be significantly reduced, even accounting for the more complicated assembly process of mounting and bonding two die in a single package, without sacrificing performance.

	GaN MMIC (Input & Output Matched to 50 Ω)	**Discrete GaN Transistor with External Matching**	**Hybrid Input-matched GaN Transistor (Input Matched to 50 Ω)**
Cost	Highest	Lowest	Medium
RF Performance	Best	Good	Better
Tuneable	Not tuneable	Input and output tuneable	Output tuneable
PCB Area	Smallest	Largest	Moderate
Customer Design Effort	None	High	Medium

Table 1: Comparison of GaN Matching Approaches

Design of the QPD1020 Hybrid Input-Matched Transistor

The QPD1020 module consists of a GaN power bar and GaAs input matching die in an SMT plastic package, as illustrated in Figure 1. An existing, commercially-proven, Qorvo GaN power bar was selected to meet the output power requirements. A suitable existing SMT plastic package measuring 6 x 5 mm was chosen, which helped reduce development timescales. Plextek RFI then designed the bespoke GaAs input matching die and bond-wire transitions to match the input of the transistor to 50 Ω at S-band.

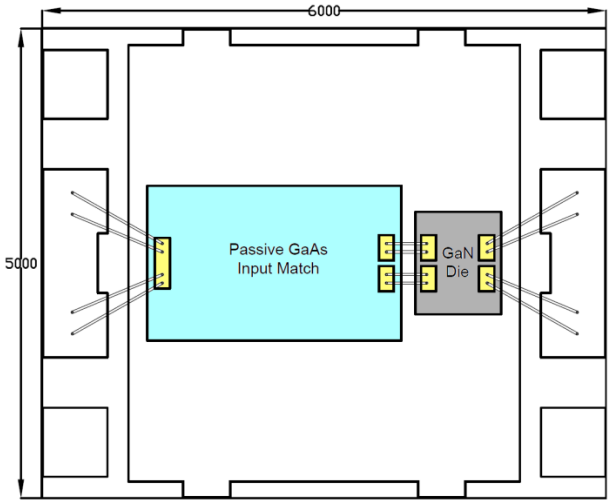

Figure 1: Internal layout of QPD1020 (dimensions in µm)

The passive GaAs die was designed to occupy the length of the package and so reduce the bondwire lengths. Similarly, the GaAs and GaN die were placed as close together as possible to minimise the bond wire length at this most critical point where the impedance is at its lowest. As can be seen in Figure 1, there is scope to reduce the size of the component through the use of an alternative custom package. Whilst shortening the length of the GaAs input matching die would have been feasible, for the selected package this would have resulted in longer bondwire lengths, which would degrade RF performance.

The input matching network has a low-pass response implemented using series transmission lines and shunt capacitors. On-chip shunt resistors are also included on the passive matching die to improve in-band stability. This reduces available gain and was therefore implemented with caution. Some additional modest off-chip stabilisation may therefore be required to ensure unconditional stability down to very low temperatures. The GaAs input matching and bondwire interface to the GaN transistor were EM-simulated and minor changes to the layout were made to compensate for the small changes in performance.

The GaN-on-SiC die was fabricated on Qorvo's high voltage 0.25 µm GaN process, which can be operated at drain bias voltages up to 50 V. The GaAs die was fabricated on a Qorvo passive process.

The QPD1020 can be operated in both pulsed and CW modes. Because of its CW capabilities, it can be used with long radar pulses. The gate biasing is implemented off-chip, which allows flexibility in the implementation of the low-frequency decoupling and allows for specific operating modes such as gate pulsing.

QPD1020 Hybrid Input-matched Transistor Measured Performance

The hybrid input-matched transistor was fabricated and the S-parameters of a number of samples were measured. Figure 2 shows the measured S-parameters of a typical part versus frequency. The input match is greater than 15 dB between 2.8 GHz and 3.6 GHz and the S_{21} is around 13 dB in-band. These measurements were made with no output matching network present and the transistor output terminated into 50 Ω. This means that the gain of amplifiers designed using the QPD1020 will

be higher than the S_{21} shown. The drain-source impedance of the transistor is largely capacitive at these frequencies and hence the unmatched output return loss appears highly reflective.

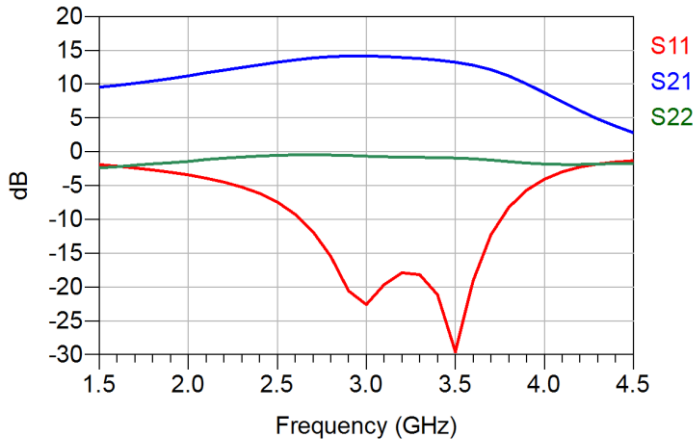

Figure 2: Measured S-Parameters of QPD1020 hybrid input-matched transistor only

Figure 3 shows load-pull measurements at 2.7 GHz (Z_0 = 33.4 Ω) with the square marker positioned at the centre of the efficiency contours. Figure 4 shows a similar set of measurements at 3.1 GHz and Figure 5 at 3.5 GHz. A summary of load-pull results is presented in Table 2.

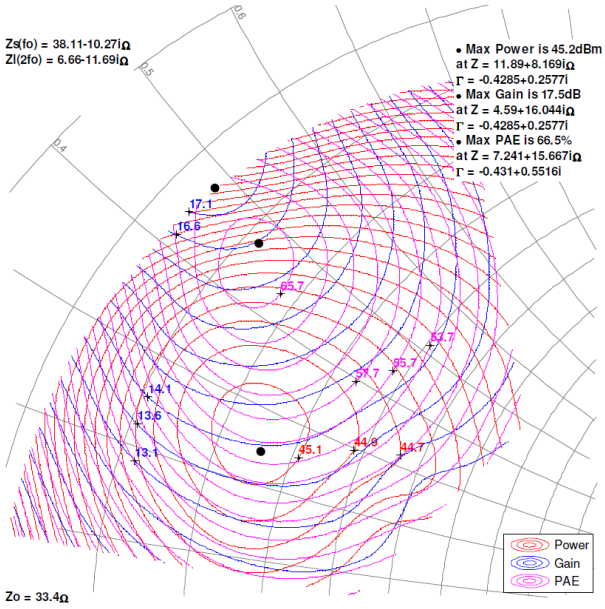

Figure 3: Load-Pull Measurements of QPD1020 hybrid input-matched transistor at 2.7 GHz

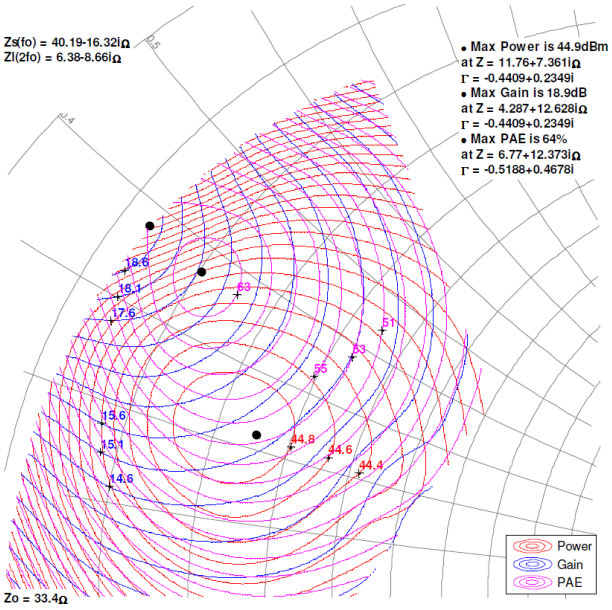

Figure 4: Load-Pull Measurements of QPD1020 hybrid input-matched transistor at 3.1 GHz

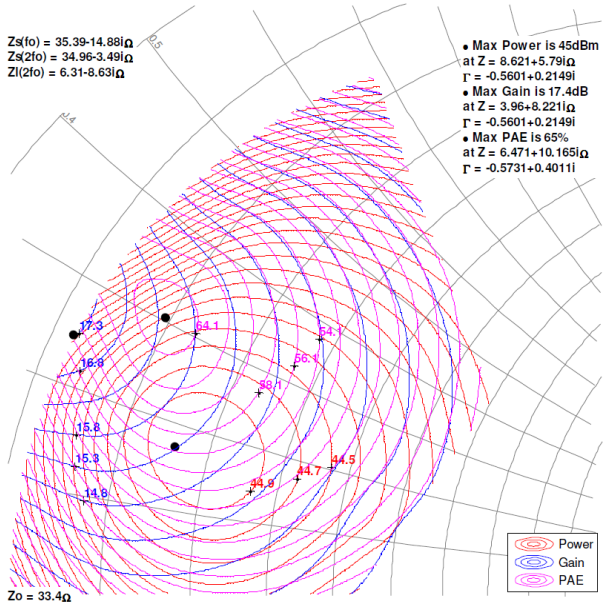

Figure 5: Load-Pull Measurements of QPD1020 hybrid input-matched transistor at 3.5 GHz

Frequency	2.7 GHz	3.1 GHz	3.5 GHz
P_{OUT} – Power Tuned	45.2 dBm	44.9 dBm	45.0 dBm
PAE – Power Tuned	55.0%	53.7%	56.7%
P_{OUT} – Efficiency Tuned	43.6 dBm	43.6 dBm	43.9 dBm
PAE – Efficiency Tuned	66.5%	64.0%	65.0%

Table 2: Summary of Load-Pull Measurements of QPD1020 hybrid input-matched transistor

Power Amplifier Design and Implementation

The measured data presented above was used to design a 2.7 – 3.1 GHz power amplifier, which is provided as a reference design for the QPD1020. A circuit schematic of the PA is shown in Figure 6.

By implementing the output matching network on the PCB, the customer has flexibility in the operation of the PA. The PA can be tuned for greater output power or efficiency depending on the end application and performance can be optimised for the required operating band. As an example of the trade-off between RF output power and efficiency, the load-pull measurements of the QPD1020 module show that at 3.1 GHz a power match would result in 44.9 dBm (30.9 W) of output power at 53.7% PAE, whereas an efficiency match would result in 43.6 dBm (22.9 W) at 64% PAE (excluding output matching losses).

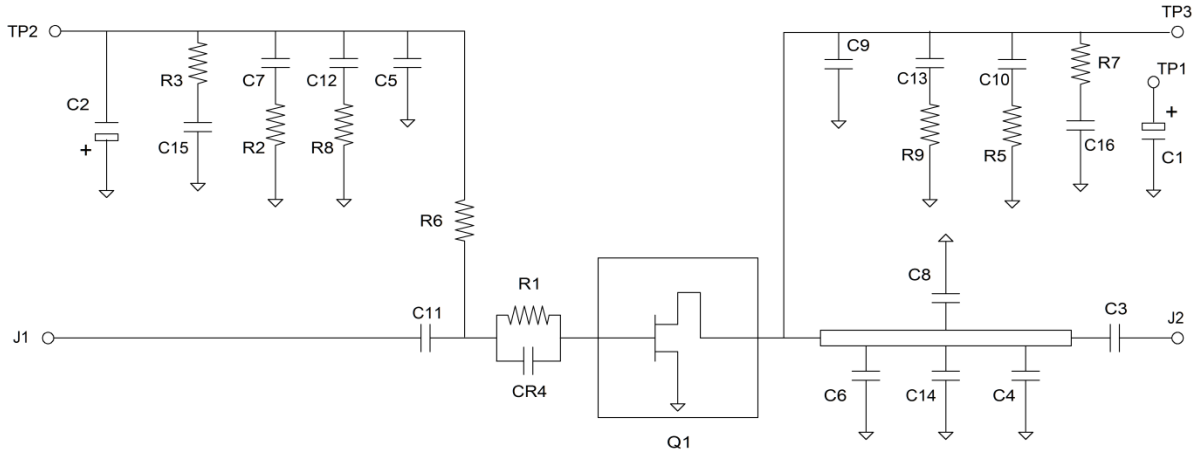

Figure 6: Schematic of the QPD1020 PA Reference Design

The output matching network of the reference design is a two-pole low-pass filter structure with an additional shunt capacitor to tune the second harmonic. Low-loss, physically small capacitors were used to reduce parasitic inductance and minimise losses. It is important to ensure that the capacitors on the output matching network can withstand high voltages necessitated by the high operating voltage of the GaN transistor.

Due to the internal input matching network, very few input matching components are required on the PCB. A DC block, a pair of stabilising resistors and a series of gate decoupling capacitors are the only components that are required. It can be seen in Figure 7 that most of the PCB at the input consists of a 50 Ω transmission line and that the PCB can be made even smaller if the banana sockets included for ease of testing were not required.

Figure 7: Photograph of the QPD1020 PA Reference Design

The PCB is constructed from Rogers 4350B laminate with a thickness of 20 mil (0.51 mm) and is bonded to an aluminium carrier. The PCB measures 40.1 x 63.0 mm (1.58" x 2.48"). The surface-mount plastic package results in simpler PCB assembly compared to traditional metal-ceramic packages. Copper-filled through-vias provide a low thermal resistance and low inductance path to the metal carrier. The temperature under the package can be measured through a hole drilled in the side of the aluminium carrier.

Power Amplifier Measured Performance

The measured S-parameters of a typical PA reference design are plotted in Figure 8. It delivers 17.5 dB of small-signal gain at 2.7 GHz and 17.9 dB at 3.1 GHz with a slight positive gain slope. The input return loss is better than 10 dB across the band, reaching 30 dB at 3.15 GHz. The design was optimised for PAE rather than for high output return loss. It can be seen that the small-signal gain is greater than 15 dB between 2.4 GHz and 3.5 GHz, demonstrating the wideband nature of the internal input matching network. Five units were tested over the temperature range -40°C to +85°C with excellent repeatability observed between the units.

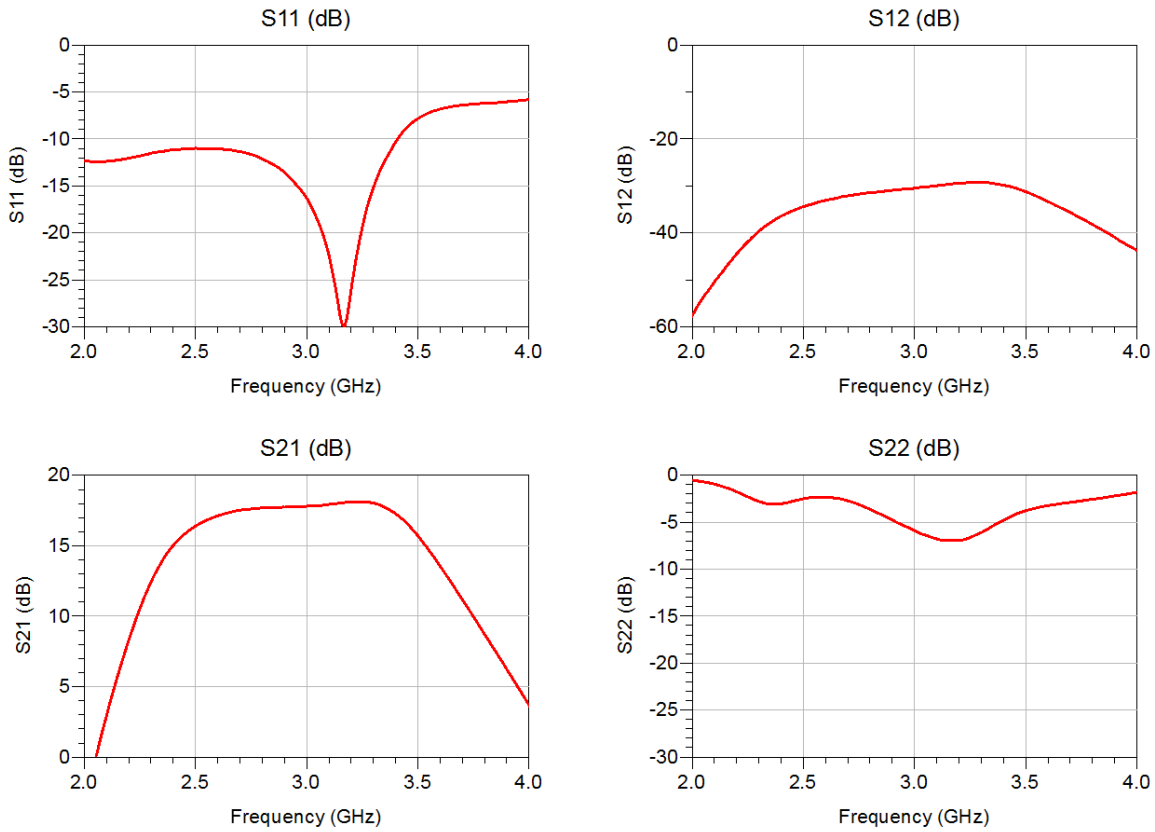

Figure 8: Measured S-parameters of QPD1020 reference design PA

The measured large signal performance of the PA across frequency and temperature is plotted in Figure 9. The output power is a minimum of 21 W with 57% efficiency at P-3dB compression and 25°C, inclusive of all matching network and connector losses. The output matching network was tuned for optimum efficiency, and it can be seen that the efficiency is flat versus frequency.

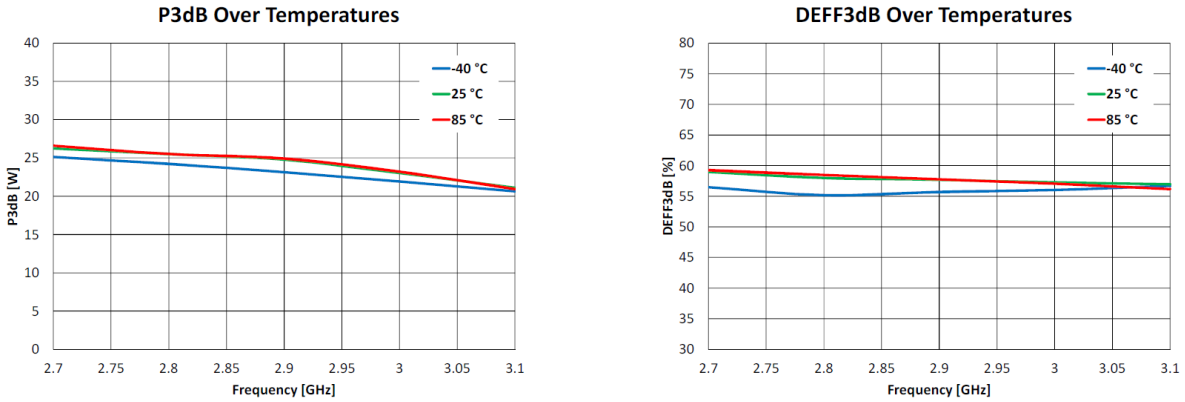

Figure 9: Output power (left) and efficiency (right) of QPD1020 reference design PA at P-3dB compression

Conclusions

The design of the Qorvo QPD1020 GaN transistor with internal GaAs input matching is described. The input matching network is designed for the 2.7 – 3.5 GHz frequency range, making the transistor suitable for S-band radar applications at a reduced cost compared to a GaN MMIC. The output matching network is implemented on the PCB to allow large-signal performance to be optimised for

a desired frequency band. High performance is demonstrated using the transistor in a reference power amplifier designed between 2.7 to 3.1 GHz. The QPD1020 can be used as an output stage in an active phased-array radar system or as a driver amplifier for a higher power output stage.

Bibliography

[1] S. Glynn and L. Devlin, “An X-band GaN PA MMIC for Phased Array Radar Applications,” in *ARMMS Conference*, 2016.

[2] R. Smith, A. Dearn and S. Glynn, “The Design of High Performance L-band GaN PAs Using Commercially Available Discrete Transistors,” in *ARMMS Conference*, Nov 2016.