Using Active Load Pull to realise Harmonic Efficiency Enhancement in MMIC Wideband Amplifiers

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Abstract—This paper emphasises the importance of including harmonic load pull in the characterisation of transistors and the benefits of integrating measurement simulation and design in a single environment. The design of a 0.5 W, 5-10 GHz GaAs pHEMT driver stage with good PAE performance, using this methodology is detailed.

Keywords – MMIC design, load pull, nonlinear design, harmonic termination, CAD modelling.

1. Introduction

The use of modern nonlinear CAD tools has been of great benefit to RF and microwave design engineers, especially those engaged in the field of power amplifier design. Coupled with this has been the increase in the availability and capability of load pull systems, which has enabled the characterisation of high power devices [1] in controlled termination impedance scenarios. There are a number of problems with the models used in such simulations; they have been largely determined under specific operating conditions and rarely do suppliers provide data on accuracy or boundary conditions. Further the initial measurements tend to be conducted on small cell size devices and scaled up, partly due to time constraints, partly due to the problems associated with measuring high power levels at the wafer level. Similarly, although load pull systems can determine the optimum impedance conditions the data gathered cannot be directly incorporated into a simulator other than for visualisation. It is now becoming possible to join these tools to enable the user to create nonlinear models of devices under conditions of their own choosing which can be directly utilised in standard nonlinear simulation software.

The limitation in device models is entirely understandable. To produce equivalent circuit models that accurately simulate the performance of active devices under all temperature, bias, frequency and drive power conditions would prove a mammoth and costly task. Add to this the requirement for scaling the device and the recent high efficiency modes incorporating 2nd, 3rd and even higher harmonic terminations and the ambition becomes totally uneconomical. The consequence of this is that designers are faced with a choice, between using models within their known accurate envelope, or trying multiple

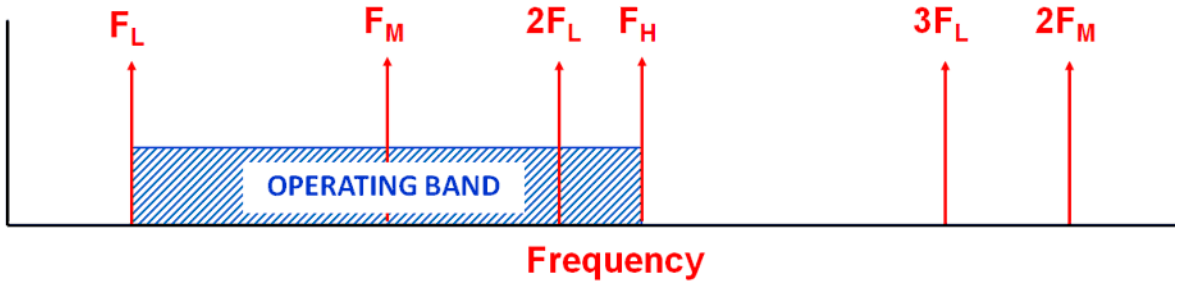


Figure 1, Harmonic positions in >octave amplifiers.

possible solutions of a design in the hope that at least one will fit the bill. Both of these have obvious draw backs, the former that the optimum solution is not possible because the device model is restricted to previously proved operating conditions and the latter is wasteful in terms of the number of iterations (wafer real estate) and design 'spins' (wafer runs) that are necessary.

One area of particular interest currently is the use of harmonic terminations to enhance performance, particularly efficiency. Many of these methods have been outlined by Cripps [2] and exemplary performance has been achieved over significant bandwidths, [3]. At higher frequencies such as X band the nonlinear model performance at the harmonics tend to do less well. There is also a practical limitation in that with ≥ octave bandwidths for the lowest frequency the 2nd harmonic will fall in band and thus the impedance will be determined by that required for the fundamental at this frequency. The problem is displayed graphically in Figure 1. In the case of an above octave amplifier the 2nd harmonic of the lowest in band frequency, $2F_L$, falls within the operating bandwidth. Therefore either higher order terminations must be utilised, or a higher in band frequency (such that $2F_X > F_H$) selected.

2. Active Load-Pull (ALP) and Waveform Engineering

The ALP system developed at Cardiff University has a number of advantages over conventional passive systems. Primarily this is concerned with the highest possible reflection coefficient that can be achieved. In passive systems this is determined by the loss between the device being measured and the tuner. Typically as frequency increases so does this loss, thus at X band and above in passive systems it is difficult to achieve a reflection coefficient, Γ, >0.8 at the fundamental and >0.6 at the 2nd harmonic.

For the ALP system the limitation in Γ is determined by the output power capability of the amplifiers in the loop. Although the cost of producing power increases with frequency, the harmonic levels themselves are usually 10-15 dB below the fundamental thus dramatically reducing the power requirements of the harmonic amplifiers. The Cardiff University system is currently equipped with 20W 2-20GHz load pull amplifiers. This enables the system to not only create the necessary conditions for high efficiency modes such as class F and J [4], but also to be capable to harmonic injection [5].

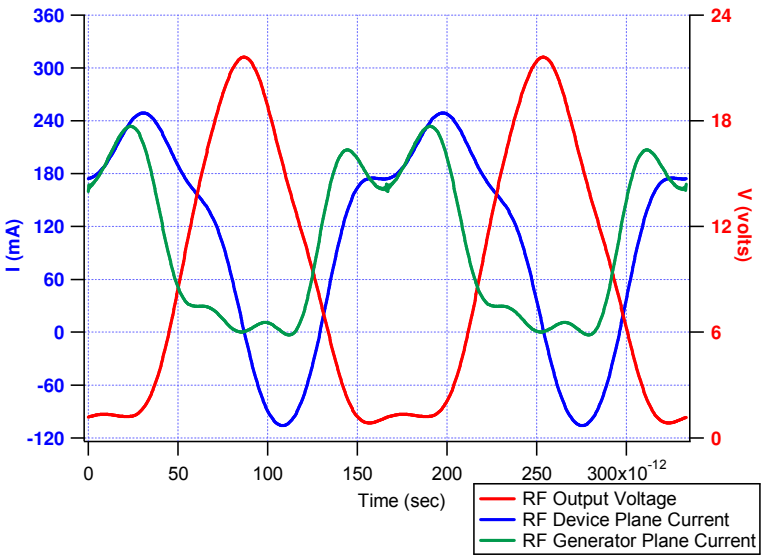


Figure 2, Voltage and current waveforms resulting from the optimised fundamental, 2nd and 3rd harmonic loads for an overdriven class A, 10x75 GaAs pHEMT at 6 GHz.

An often overlooked advantage of the ALP system is that that at frequencies other than the test signals the device 'sees' a 50Ω termination. Hence its behaviour is not affected by high levels of reflected noise as can be the case in some other load pull systems.

The term waveform engineering comes from the ability of the system operator to construct desired waveform shapes by altering the phase and magnitude of the fundamental and harmonic loads. The control software for the system allows not only feed networks, but also intrinsic parasitic

elements to be de-embedded such that the voltage and current waveforms at the current generator plane can be observed, Figure 2.

3. Overview of the Proposed Design Process

To maximise the benefits offered by the waveform engineering system, rather being a front-end part of the design process it properly belongs as an integrated part of the design flow, linked in with the CAD software role. The measurement system is first used to understand the behaviour of the device and determine if it is suitable, or the best choice, for an application, and if so then to determine the optimum operating conditions. This is referred to as the "Measure" phase in Figure 3. When dealing with devices at the wafer level it is not necessary to conduct measurements at a large number of frequencies even for wideband applications due to the consistent nature of the device characteristic trajectories [6].

Having characterised the device the captured data is made available to the CAD software by storing the data in the industry standard MDIF (Measurement Data Interchange Format) file structure [7]. The data; input current, output current and voltage at each harmonic is referenced by load impedance, input voltage, bias voltages, temperature, etc. An attraction of this approach is that the file can be added to as more measurements are taken, and so it is not necessary to capture all of the impedance information for each fundamental load impedance; an approach which would lead to an 'explosion' in the amount of data captured and most of it would be redundant.

In wideband applications it is unlikely that the matching impedance network synthesised will achieve exactly the required response. Hence it is advantageous to be able to understand the implications, particularly of what out of band terminations have on the device, by testing the performance in this impedance environment. It is impractical to create a DLUT model of every combination of fundamental and harmonic load; the vast majority of the data will be redundant. In practice it is likely that the loop CAD-Measure-Assess, will be repeated several times as the matching circuit complexity is increased as it closes in on the best solution, i.e. as parasitics and Electro-Magnetic (E-M) simulations are added.

When the device in the measurement system with the loads from the CAD simulation produces a satisfactory performance the design moves to the finalised layout and manufacture. It may be that at this stage further frequencies will be checked as a final confidence measure.

A further advantage of this approach becomes clear at this stage; the amplifier design has been done without reference to any device data from the foundry, thus showing how the approach can be used for new technologies before sufficient data has been generated to produce more conventional models.

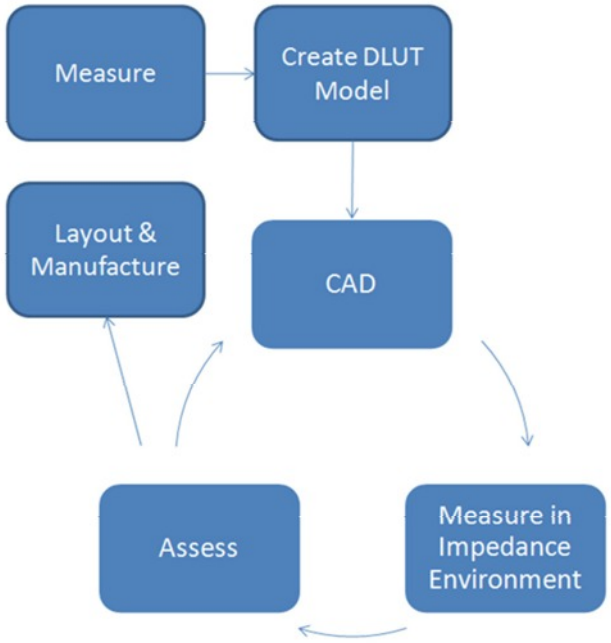


Figure 3, Flow Diagram of Waveform Engineering Design Process.

4. Demonstration of the Waveform Engineering Based Design Process

To demonstrate this process the design of the output matching network for a 5-10 GHz 0.5W driver stage was undertaken. The requirement was for the device to be driven in class A and be operated between P1dB and P3dB, i.e. in the highly nonlinear region. A key objective was to maximise Power Added Efficiency (PAE), aiming to achieve >40% across the bandwidth.

In line with the described process the device was initially biased in class A and load pull measurements were conducted across the frequency and input power range to determine the optimum load points at each frequency and the performance that could be achieved. These are summarised in Table 1.

Freq. (GHz)	Γ_L (Mag/Ang)	PAE (%)	Pout (dBm)	Gain (dB)
4	0.26/44.6°	49.2	27.4	21.1
6	0.35/65.9°	51.4	27.7	15.0
8	0.52/80.8°	51.2	27.0	13.5
12	0.54/104.1°	44.5	27.2	10.8

Table 1, Measured optimum PAE loads and performance

It has been established [2] that harmonic terminations can be used to improve the PAE of RF power amplifiers. The theory behind these modes is based upon class B operation of the device. It was suggested that a similar condition existed for class A. Terminating the device with the optimum load impedance at 6GHz a 2nd harmonic load pull was implemented. This showed that the impact of the 2nd harmonic load impedance could be ~±10% on the PAE as shown in Figure 4. This graphical representation is useful to the designer as they can visualise the efficiency benefits of 'steering' the out of band impedance.

Using this information and fundamental optimum load impedances a matching circuit was tested that would attempt to get the band edges close to the optimum loads whilst targeting the 2nd harmonic of 6GHz (chosen as the 2nd harmonic would be close to the top frequency, but far enough away to effect a substantial impedance change) on the region of highest efficiency improvement. Note that the power and efficiency levels recorded are at the device plane and hence an allowance needs to be made for the insertion loss of the output matching circuit.

Broad bandwidth design is about balancing conflicting objectives. In order to come as close as possible to the ideal impedances multiple matching sections are required, however this increases insertion loss and hence has a detrimental impact on efficiency and power. A compromise is necessary which provides adequate overall performance. To achieve this it is extremely helpful to work within the CAD environment with the DLUT model, where the device and circuit losses can be examined together.

This graphical representation is useful to the designer as they can visualise the efficiency benefits of 'steering' the out of band impedance. Note that the measurement grid extends beyond the real impedance plane and is equivalent to harmonic injection. The positive benefits of the 2nd harmonic termination are equally clear as summarised in Table 2, (note that this is the improvement at the optimum grid point – it is clear from Figure 4 that

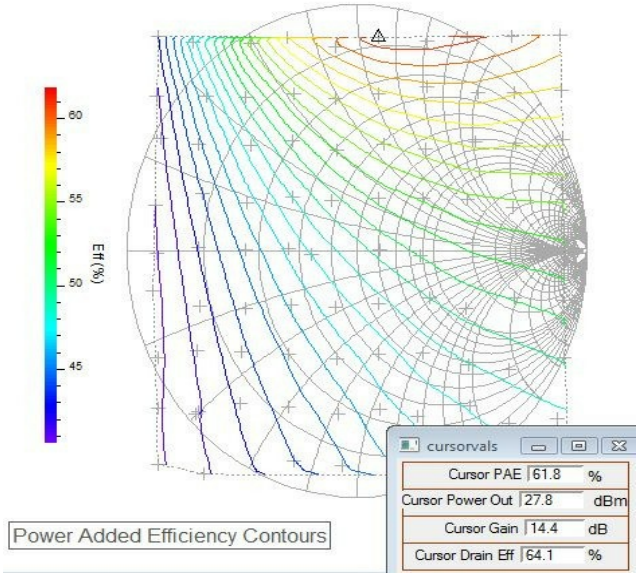


Figure 4, 2nd harmonic load pull across the impedance plane plane with the fundamental terminated at the optimum PAE load.

there is 'still more to be had' above the measurement grid).

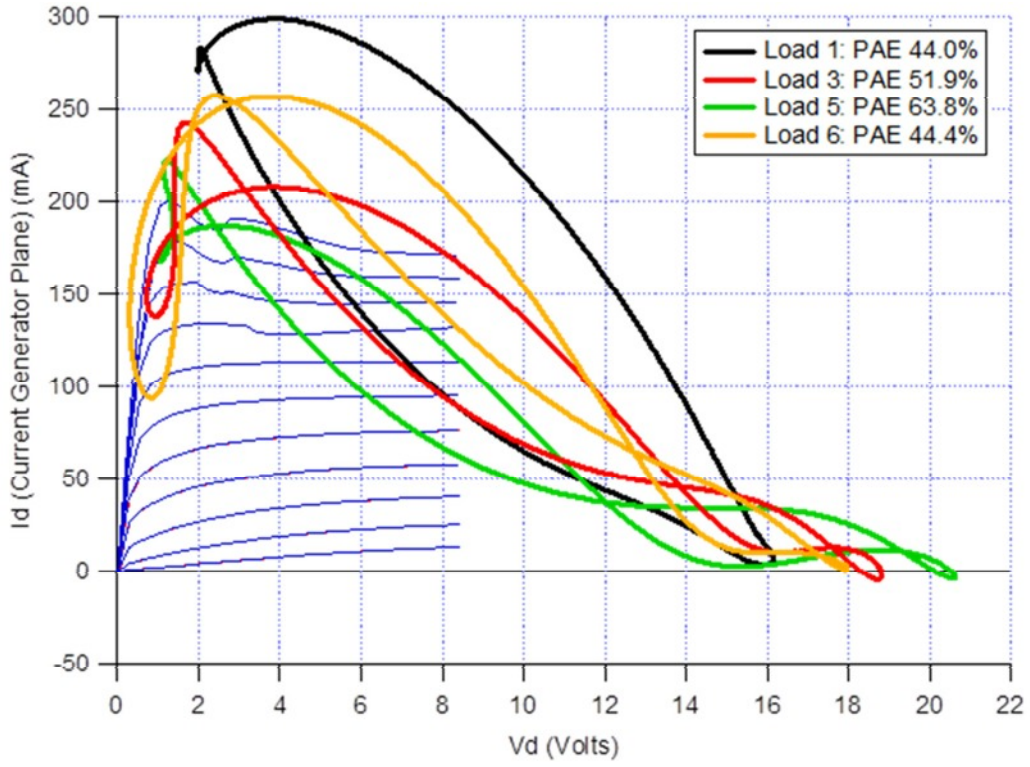
Γ_2 Load (Mag/Ang)	P_{IN} – Avail. (dBm)	P_{OUT} (dBm)	PAE (%)	Max. Gain (dB)	Av. Gain (dB)	P_{OUT} 2^{nd} H (dBm)	P_{OUT} 3^{rd} H (dBm)
0.0/_0°	18.1	27.6	51.0	15.9	9.5	7.5	10.8
0.89/_79°	18.1	27.9	58.8	16.5	9.8	4.0	6.2
	Improvement:	0.3	7.8	0.6	0.3	3.5	2.6
Table 2, Performance improvements from 2nd harmonic tuning at a fundamental frequency of 6GHz.							

An important point to note is that over about 50% of the impedance plane the 2^{nd} harmonic has a negative impact on the PAE performance. A similar plot of the output power contours revealed a power variation across the real impedance plane is ±0.5dB. This clearly shows that whether or not harmonic enhancement is used the impact should not be ignored. An investigation of the 3^{rd} harmonic termination effects revealed that is had <4% change in PAE, and also the optimum point moves across the impedance plane depending upon the drive power level.

Observing the dynamic loadline at 6GHz Figure 2, it is clear that as the harmonic tuning improves the PAE the dynamic loadlines moves from being approximately centred on the bias point (9V, 150mA) and moves towards what would be expected from a more class B loadline. The performance at each load is summarised in Table 3. It is also seen that in the case of the worst case harmonic loads (Load 6), the effect of the harmonic waveform engineering is to shift the load line to the left such that it is limited by the knee voltage of the device, whereas with the optimum terminations the loadline is shifted to right and less is incident upon the knee and higher peak voltages are achieved. Consistent with loadline theory [8] more efficient performance equates to a higher resistance load (reduced slope on the load line).

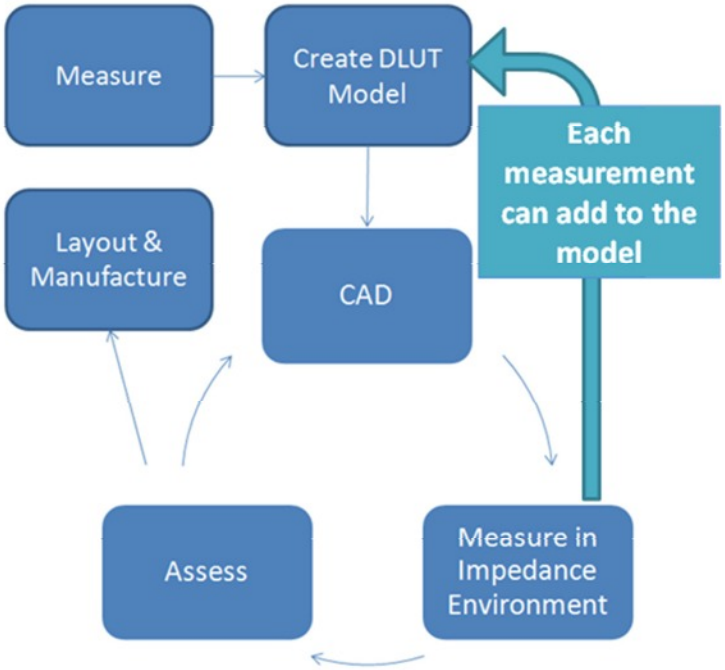
Name	Description	Γ_1 (Mag/Pha)	Γ_2 (Mag/Pha)	Γ_3 (Mag/Pha)	PAE (%)	Pout (dBm)	Gain (dB)
Load 1	50Ω F1 F2 F3	0.09/ 82.6°	0.02/ -116.0°	0.02/ 158.8°	44.0	27.7	14.3
Load 2	Theory F1 50Ω F2 F3	0.23/ 108.9°	0.01/ -179.4°	0.01/ 38.8°	44.8	27.6	14.7
Load 3	Opt F1 50Ω F2 F3	0.42/ 68.1°	0.01/ 171.0°	0.01/ 121.2°	51.9	27.1	15.3
Load 4	Opt F1 F2 50Ω F3	0.42/ 68.1°	0.90/ 72.3°	0.00/ -22.5°	61.4	27.6	16.1
Load 5	Opt F1 F2 F3	0.42/ 65.9°	0.90/ 89.3°	0.86/ -132.1°	63.8	27.7	16.6
Load 6	Opt F1 Worst F2 F3	0.42/ 65.9°	0.87/ -170.4°	0.50/ -152.6°	44.4	26.6	14.8
Table 3, Summary of harmonic loads and associated performance on 10x75 device at 9V 150mA bias. Note Loads 2 & 4 are not plotted for clarity.							

It is important to remember that the fundamental load has been kept constant except for Loads 1 & 2. For the others the change in the loadline is purely as a result in the change in harmonic impedances.

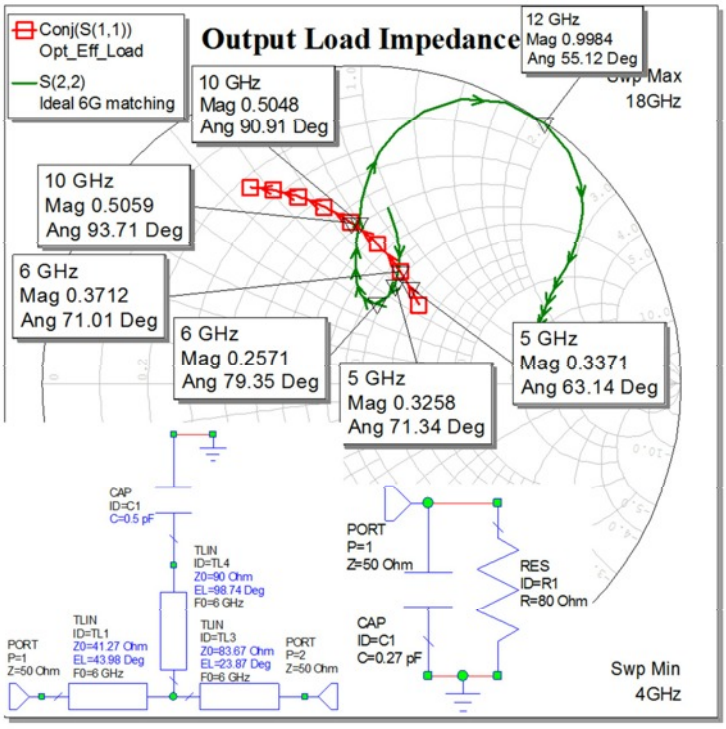


It is also worth noting that a good check of whether the right value of the output capacitance has been chosen is to see whether all of the negative drain current has been removed by the de-embedding.

In this case therefore the process has started with measuring the optimum fundamental loads and then measuring the harmonic performance at these optimum impedances; creating a DLUT model from the measured data. Within the CAD environment the load equivalent circuit and simple transmission line models are used for the initial matching circuit design as a first approximation of the solution. These are optimised such that the load matches the equivalent circuit at the band edges and the harmonic termination at 6 GHz is close to the measured optimum at near 1/_80°. With each set of measurements data is added to the model, thus its comprehensiveness increases with each data set acquired, Figure 5.

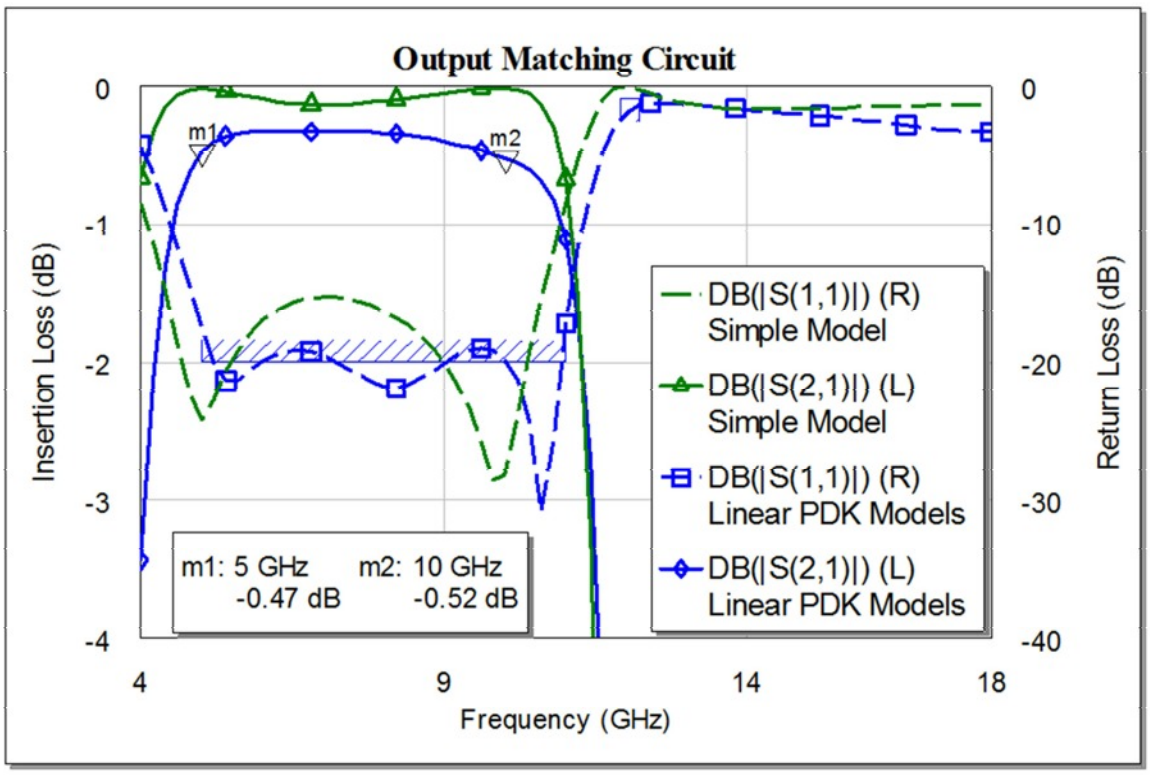


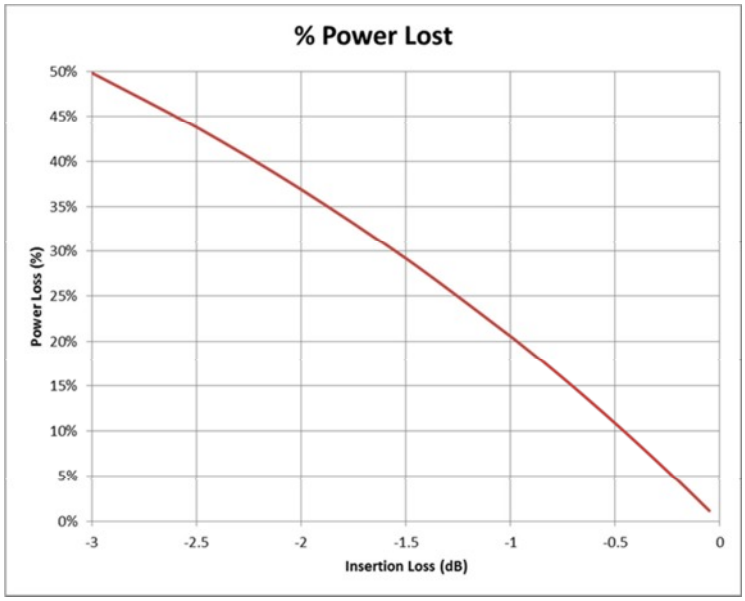
The first pass solution is shown in Figure 8. Although the angle of the harmonic is not exactly right until the improved circuit models are included it is a satisfactory start. An advantage of this matching



topology is that drain bias could be incorporated at the end of the capacitor coupled stub.

The next iteration of the matching circuit includes discontinuities for the 'Tee' junction and the microstrip line models for the GaAs substrate. To increase the accuracy of the model an additional frequency (10GHz) was added using these latest loads. At this frequency with a load reflection coefficient of 0.43/_84° the device will deliver an output power of 27.4 at a PAE of 43% and a maximum gain of 11.5dB. The loss of the output matching circuit needs to be calculated to see whether this will meet the target of 40% PAE and 27dBm output power. The insertion loss simulation is shown in Figure 7, a comparison with the PDK device output impedance is given. At this stage we are still working with the equivalent output circuit model as we only have a limited



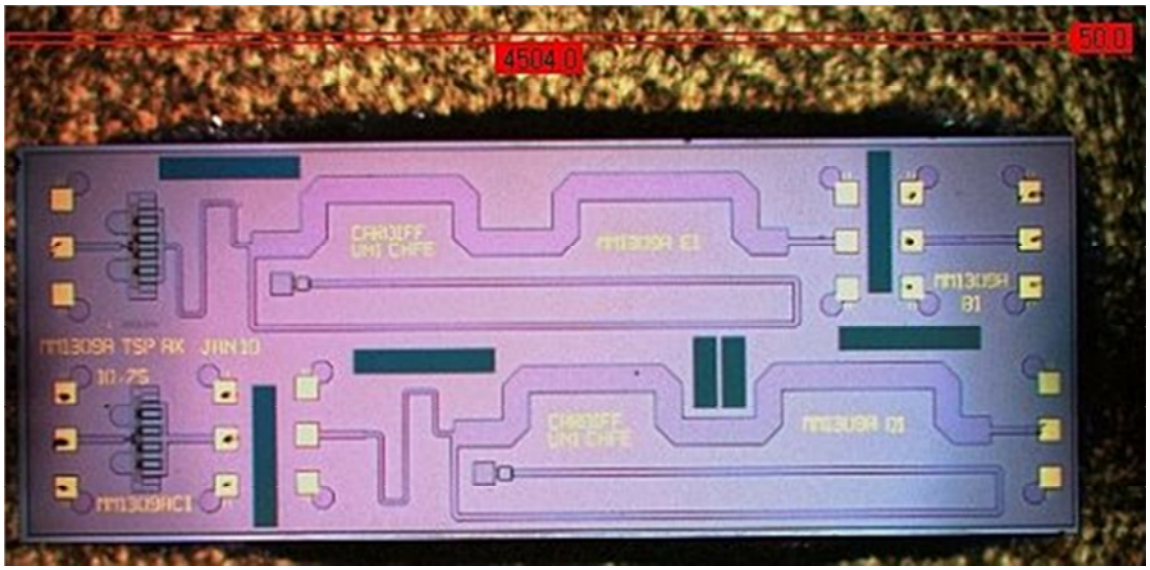


frequency step in the DLUT model. When designing the output matching network it is useful to keep in mind the effect on performance that the insertion loss will have. As shown in Figure 9 0.5dB of insertion loss equates to over 10% in power.

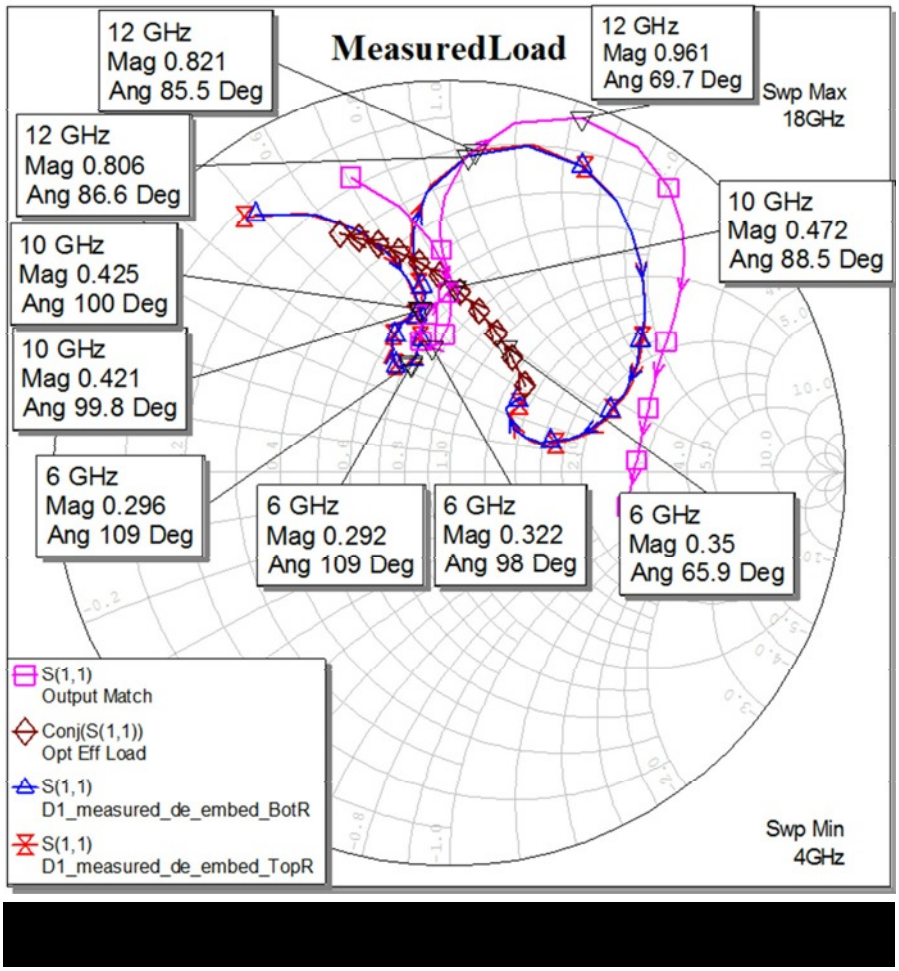
The manufactured test cell is shown in Figure 10. This cell contains a de-embedding circuit consisting of two feed lines back to back, device and output matching circuit on their own, and the device with output matching. In this case no input matching was included in order to make the most accurate comparison between the individual device and the output matched one.

The measurement of the output matching network, Figure 11, show that although we have been concentrating on active device modelling there is still some way to go with the passives! The discrepancy was in fact traced to the high frequency model of the capacitors.

The performance of the manufactured MMIC at 6 GHz is shown in Figure 12. It can be seen that at

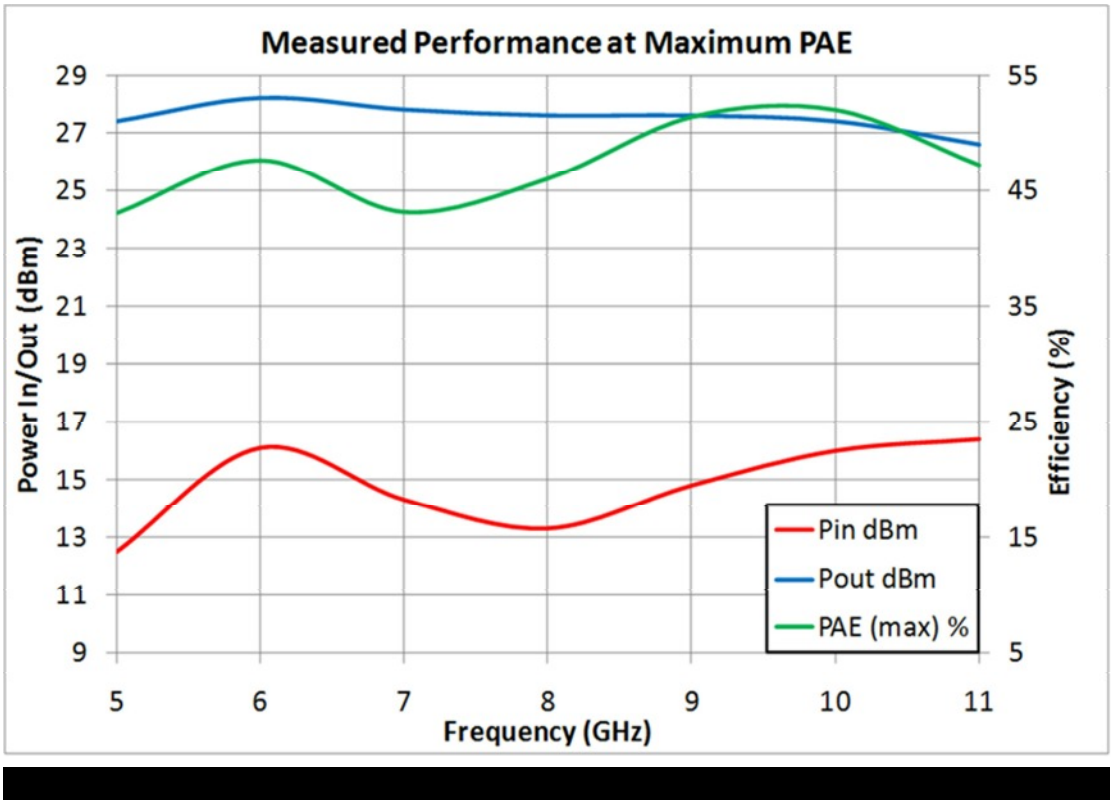


the peak a PAE of 49% at an output power of 28.1 dBm was achieved. A clear increase in the PAE at 6GHz can be observed, despite the fact that as shown in Figure 11, the fundamental impedance is moving away from the optimum. This increase is attributed to the harmonic termination.



The advantage of including a device in the manufactured wafer cell is that its performance can be measured and compared with that of the device in the original design. Although there is no guarantee that the performance will be the same as the device in the matched circuit it is likely to be closer than the original device, due to their proximity and shared processing. A load pull analysis of the manufactured device determined its optimum PAE load and associated performance. The more recent device had a slightly higher PAE accounts for achieving an acceptable PAE in the MMIC despite the higher insertion loss of the matching circuit.

It should be noted that the calculation of PAE uses Maximum Available Gain (MAG) thereby assuming that the optimum input matching will be achieved. This is done as it gives the designer the knowledge of what is the best performance that can be achieved, and is the approach commonly adopted in CAD. A lower limit for PAE could be calculated using the Available Gain (GAV). In practice the input match will often be designed such that for a fixed input power level with frequency the required drive level for optimum PAE will be delivered to the device, whilst maximising the gain where possible.



5. Conclusion

It is clear from the performance that an enhancement in the PAE results from the 2nd harmonic load impedance, as expected. The peaking of the PAE at the lower part of the pass band can clearly be seen in Figure 12, despite the fundamental load impedance being further from the optimum load (Figure 11). In wide bandwidth applications this approach allows for conventional optimisation of the load impedance at one part of the frequency band and then to 'pick up' the performance elsewhere in the frequency range using harmonic enhancement. This effect has been used in narrower bandwidth applications [4], but the method described here uses a graphical approach based on ALP measurement data, rather than attempting to construct a particular class of operation.

By making the measurement system an integral part of the design process a high degree of confidence in the simulation results is achieved, and provided the passive circuit elements can be accurately modelled it is possible to achieve performance from the CAD in the manufactured circuits.

Further work [9] on the DLUT modelling approach is working towards replacing the measured data grid with polynomial coefficients which describe the power waves as a function of load impedance and input drive. This will not only greatly reduce the size of the data table, but also the relative number of measurement points as these only need to be sufficient to describe an ellipse. This increases the practicality of conducting measurements over greater power, frequency and harmonic termination ranges. It is believed that this approach may also provide a solution to the problem of yield analysis by looking at the variation in the magnitudes of the polynomial coefficients thus a basis for Monte Carlo tolerance investigation exists.

6. Acknowledgment

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