GaN HEMT vs GaAs MESFET - Practical Design Comparison

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In the recent years wide bandgap transistors (SiC MESFETs and GaN HEMTs) have appeared on the market for high power RF/microwave transistors. They offer higher power density and higher voltage operation, which in turn are associated with much lower parasitic capacitances and much higher load-line dynamic resistance, and hence wider bandwidth applications. Of the two kinds the GaN HEMTs offer higher gain performance.

This article compares the performance of a 10W GaAS MESFET which has been very popular for years and a new 10W GaN HEMT by describing the practical design of 10W Class A amplifier stages with the two transistors.

The Comparative Design Problem

The comparative designs were provoked by the fact that both of these transistors are Eudyna products (the GaAS MESFET is FLL120MK and the GaN HEMT is EGN010MK) and that they exhibit very similar output power performance. Their metal-ceramic cases are also the same. Nonlinear models are also available for both transistors. The model for FLL120MK was purchased for a modest price from Modelithics. There was already an indication that this model is well behaved [1]. The model for the EGN010MK is available for free from Eudyna and was developed by Auriga Measurement Systems.

By simply looking at the data sheets it is obvious that the GaN transistor is useful to much higher frequencies. The comparative designs though are done at around 2GHz searching to maximize the bandwidth and the gain for each transistor at the same output power (P1dB).

The design procedures are very similar to the ones described in [2] and [3]. As before, two CAD programs - MultiMatch Amplifier Design Wizard and AWR's Microwave Office – were again used in tandem.

The GaAs MESFET Design

The nonlinear model of FLL120MK was used first in Microwave Office to evaluate the maximum P1dB that could be achieved. This was done by using the tuners in the same way as described in [2]. That showed a maximum P1dB of 40.5dBm at around 2GHz (bias point: 10V, 2.2A).

Having a nonlinear model it would be possible to follow a design procedure similar to the one in [2], which started with extracting the optimum P1dB output impedances for a number of frequencies by using the tuner at the output, and then using these impedances in MultiMatch to synthesize a network to provide them. That network could then be brought back into Microwave Office to check and tune the performance.

However, it was decided that because the performance would be a compromise between bandwidth and P1dB, a procedure similar to the one in [3] should be used. This design procedure uses the Power Parameters ([4], [5], [3]) of MultiMatch which provide flexibility and versatility when looking for optimum P1dB performance in a desired bandwidth.

In order to follow this procedure, an S-parameters data file was generated first by using the nonlinear model in Microwave Office. This file was then used in MultiMatch to fit a linear model to the S-parameters, which together with defined I/V Curve Boundaries and bias point, allows MultiMatch to calculate the power performance. The model fitted is used to generate the required Power Parameters. Figures 1 and 2 show the component values of the fitted linear model and graphs of the S-parameters of the model and the measured S-parameters. Note the tight fit between the two sets of S-parameters.

The model extraction was done inside the Transistor/Device Modification Module of MultiMatch. The model fitting was followed by a general analysis of the capabilities of the transistor. The results are shown in Tables 1 and 2.

Before anything else first the stability of the amplifier stage should be considered. In this case, because the transistor k-factor (Table 1) shows unconditional stability (>1) above about 1.4GHz, it was decided to synthesize the output and input networks first and then add an input shunt resistor, at an appropriate place, to take care of the instability at the lower frequencies.

Table 2 shows the maximum Output Power (Po_{max}) obtainable before the intrinsic output current or voltage starts to clip. This power is a close estimate of the maximum P1dB of the transistor,

but more importantly the output impedance and the Load-Pull Contours for this unclipped Po_{max} are the same as those for $P1dB_{max}$ ([6], [7], [4], [5]). Normally Po simulated by MultiMatch should be slightly lower than the actual P1dB or the P1dB simulated with a nonlinear model. At the P1dB point on the compression curve there is already some clipping. Table 1 also shows the optimum impedance (Z_{Lopt}) at which Po_{max} ($P1dB_{max}$) is achieved and the associated maximum power gain (Gp_{max}). Gp_{max} is the power gain of the transistor when its output is matched for Po_{max} and its input for maximum input Return Loss (RL_{in}).

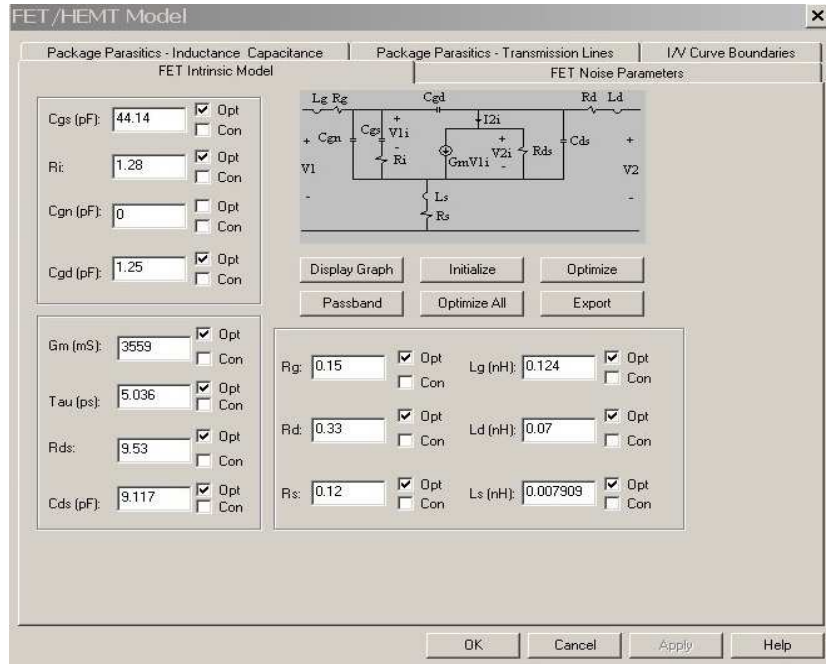

Figure 1. GaAs MESFET linear model

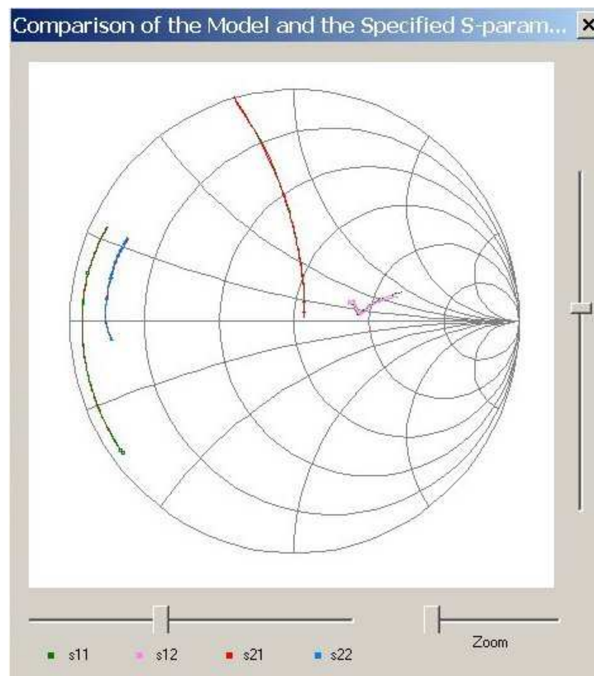

Figure 2. Graph showing the result of the fitting

FREQUENCY (GHz)	k -	MAG (dB)	MSG (dB)	Ga (dB)	Gw (dB)	GT (dB)
100.0000E-3	0.08	infinity	32.65	29.19	34.55	24.39
151.2341E-3	0.12	infinity	30.65	26.13	30.95	21.04
199.2583E-3	0.15	infinity	29.45	23.93	28.56	18.73
301.3467E-3	0.23	infinity	27.65	20.49	24.97	15.21
397.0388E-3	0.31	infinity	26.42	18.15	22.58	12.85
499.6184E-3	0.38	infinity	25.44	16.20	20.60	10.88
600.4581E-3	0.46	infinity	24.61	14.63	19.01	9.30
791.1329E-3	0.60	infinity	23.39	12.30	16.64	6.96
908.0980E-3	0.68	infinity	22.77	11.14	15.47	5.80
995.5313E-3	0.75	infinity	22.39	10.38	14.69	5.03
1.14270	0.85	infinity	21.74	9.24	13.52	3.90
1.19650	0.90	infinity	21.55	8.86	13.13	3.52
1.31170	0.96	infinity	21.10	8.12	12.36	2.78
1.37340	1.00	20.56	20.56	7.75	11.98	2.41
1.43790	1.04	19.36	19.36	7.38	11.60	2.05
1.50560	1.09	18.63	18.63	7.02	11.23	1.69
1.57640	1.13	18.01	18.01	6.66	10.85	1.34
1.65050	1.17	17.49	17.49	6.31	10.48	1.00
1.72820	1.22	16.95	16.95	5.96	10.11	0.66
1.80950	1.26	16.46	16.46	5.62	9.75	0.32
1.89460	1.29	16.01	16.01	5.28	9.39	-0.00
1.98370	1.34	15.53	15.53	4.94	9.03	-0.32
2.07700	1.38	15.08	15.08	4.62	8.68	-0.62
2.17470	1.41	14.66	14.66	4.30	8.33	-0.92
2.27700	1.45	14.24	14.24	4.00	7.99	-1.19
2.38410	1.48	13.82	13.82	3.70	7.66	-1.45
2.49620	1.51	13.41	13.41	3.41	7.33	-1.70
2.61360	1.53	13.01	13.01	3.13	7.02	-1.93
2.73650	1.54	12.63	12.63	2.88	6.72	-2.12
2.86520	1.56	12.26	12.26	2.64	6.44	-2.29
3.00000	1.57	11.87	11.87	2.41	6.16	-2.44

Table 1. GaAs MESFET k-*factor* and Gain

FREQUENCY (GHz)	LOAD TERMINATION (Ohm)		OUTPUT POWER (dBm)	POWER GAIN (dB)
1.43790	3.65	-j3.87	39.669	17.688
1.50560	3.62	-j4.11	39.665	17.298
1.57640	3.59	-j4.36	39.661	16.897
1.65050	3.57	-j4.64	39.656	16.499
1.72820	3.54	-j4.93	39.650	16.103
1.80950	3.65	-j5.32	39.660	15.665
1.89460	3.90	-j5.79	39.668	15.225
1.98370	3.47	-j5.98	39.630	14.888
2.07700	3.45	-j6.40	39.622	14.505
2.17470	3.43	-j6.85	39.612	14.089
2.27700	3.42	-j7.35	39.602	13.700
2.38410	3.41	-j7.90	39.590	13.302

Table 2. ZL_{opt}, Po and Gp

The next few steps of the design procedure follow closely the procedure described in [1]. It was decided to try and see what Po could be achieved in the frequency band of 1.8-2GHz. The MultiMatch command for synthesis of a network which provides the optimum impedance for Po_{max} was invoked and that starts an impedance set-up wizard. One of the steps of the wizard's procedure shows in graphical form (Figure 3) the Load-Pull contours of Po (P1dB). The blue line in the middle of the ellipsoids represents the optimum impedances (ZL_{opt}) at which Po_{max} is achieved. The ellipsoid contours are spaced and grouped for 1dB and 2dB less power. The different colour of each individual contour in each group represents a different frequency. (The magenta line shown represents the impedances for maximum gain. If these impedances are presented to the output of the transistor then the gain will be the maximum possible, but Po will be more than 2dB less than the maximum.) The purpose of this wizard is to set the target impedance for the synthesis which in this case was set to be ZL_{opt}.

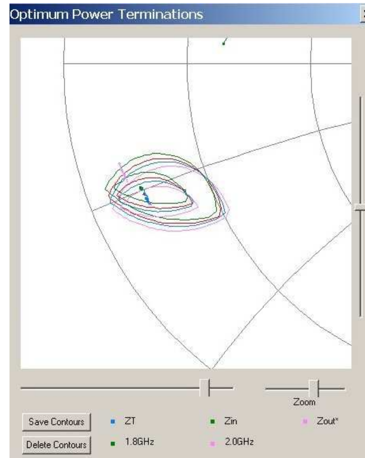

Figure 3. GaAs MESFET Load-Pull Contours for Po/P1dB

A number of iterations were then run in the network synthesis module of MultiMatch with different main-line (series) impedances to arrive at the highest Po with the most tolerance insensitive network behaviour. This capability of MultiMatch to provide immediate tolerance sensitivity evaluation of the multiple synthesis choices presented to the designer is a strong advantage. It increases the chances very substantially that the design iteration will be successful when a yield analysis is done at the end of the full design cycle. The chosen solution of the synthesis session was transferred to the analysis module where the analysis showed Po just 0.3-0.5dB lower than Po_{max}. The input matching network was synthesized next and Figure 4 shows the resulting layout of the MultiMatch solution.

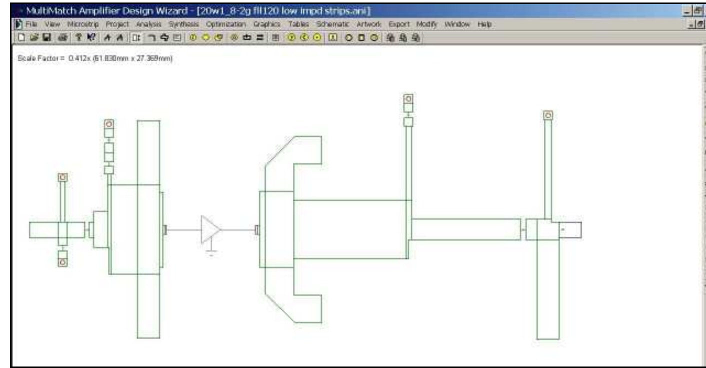

Figure 4. The first MultiMatch layout solution for the GaAs MESFET stage

This layout was translated into Microwave Office schematic and layout, and then, as described in [3], electromagnetic analysis and tuning were attempted to compensate for the effects of the microstrip discontinuities. When this design was done, MultiMatch discontinuities models were of the closed-form type based on models from the literature and they could not fully compensate for the discontinuities effects of this very high dimensions ratio layout which is typically necessary with high power amplifiers. In this case it turned out that the discontinuities effects could not be tuned out for the whole bandwidth of 1.8-2GHz. This bandwidth is more than twice wider in percentage than the design bandwidth in [3] (2.1-2.2GHz).

It was obvious that the solution of the problem should be sought in reducing the width of the main-line (series) microstrip lines, although this would bring more tolerance sensitivity. The widest lines were set to be 3mm because in Microwave Office the standard electromagnetically solved discontinuity X-models range allows width to height ratios (W/H) up to 4.0. W is the microstrip line width and H is the substrate height which in this case is 0.762mm (30mil) with Er=3.38. The newly synthesized MultiMatch design showed good performance and when translated into Microwave Office only very minor tuning was necessary for optimum performance. Because the discontinuities X-models were used it was decided not to perform an electromagnetic simulation of the layout. Figure 5 shows the layout of this design iteration in Microwave Office and Figure 6 shows the simulated P1dB.

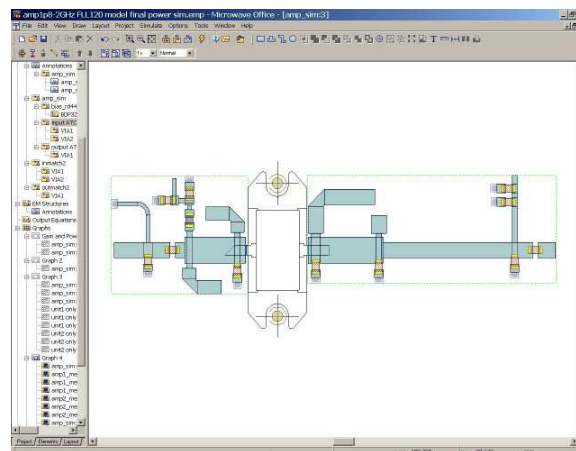

Figure 5. Final GaAs MESFET stage layout

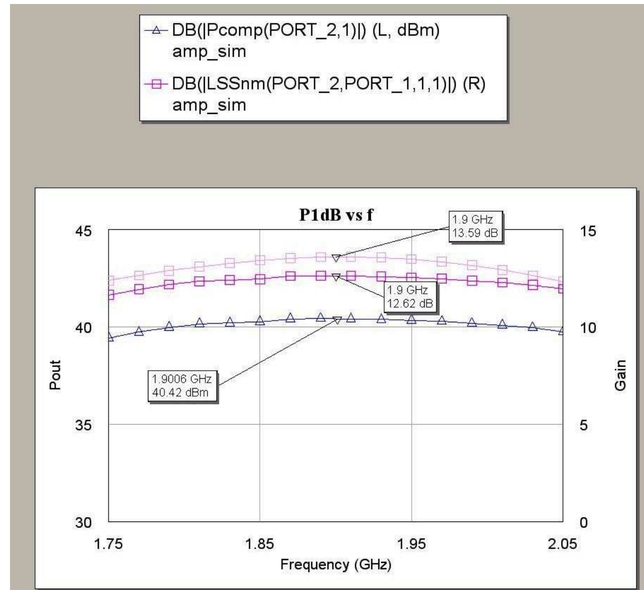

Figure 6. P1dB simulation

Two test units were built and measured. Figure 7 shows the comparison between the simulated and measured performance for Gain and RL.

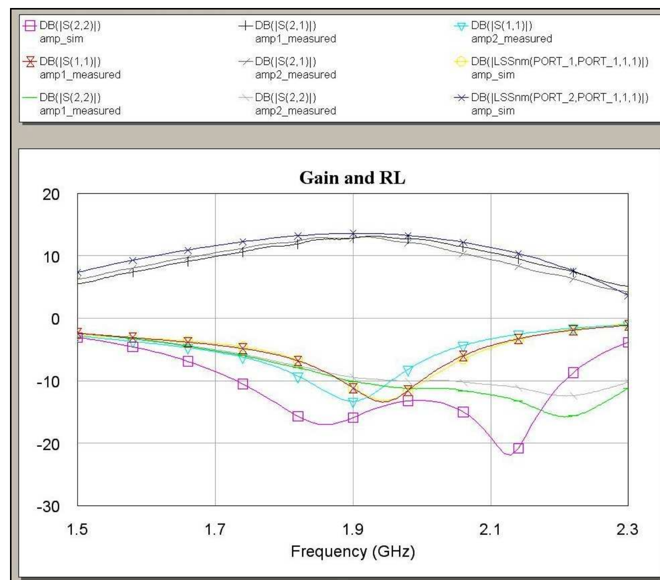

Figure 7. Gain and RL comparison

The somewhat different output RL did not affect the P1dB measured performance. It was startlingly the same as the simulated P1dB. The simulated Output IP3 is 55.5dBm and the measured values are 55.8dBm and 58dBm for the two different units which is also a very close agreement.

The designed stage was used to design a balanced stage to which a balanced 5W driver was added to realize a 20W Class A amplifier with very high linearity performance (OIP3≥58dBm). It has consistently come out of production without any necessity to tune.

It should be mentioned here that substrate specific X-models for wider lines could have been generated using the X-model development facility provided in Microwave Office, and then more iterations could be run between MultiMatch and Microwave Office to see if there was not a solution with wider main-line (series) lines (lower characteristic impedances) which would still work for the 1.8-2GHz bandwidth, but would also provide less tolerance sensitivity. This of course would have taken more design time.

At the time of writing this paper MultiMatch acquired a new discontinuity modelling module in which substrate specific models can be developed by the user in a similar manner as the X-model facility of Microwave Office. For the MultiMatch discontinuities model development though, a third party 2.5D electromagnetic simulator has to be used and instead of a data base to be filled as in Microwave Office, coefficients for polynomial curve fits of the components in pre-determined equivalent circuits must be provided. It is the Microwave Office X-models facility that provides in the fastest manner the information for the MultiMatch discontinuity models.

The MultiMatch discontinuity modelling module has already been tested up to 50GHz. It is a time consuming operation to produce substrate specific discontinuity models, but when it is done it is usually not necessary to run multiple iterations between MultiMatch and Microwave Office to compensate for the discontinuities effects.

The GaN HEMT Design

The design of the stage with the GaN HEMT proceeded in a very similar manner though with some important differences. First, simulations with the nonlinear model using tuners in Microwave Office showed maximum P1dB of 40.6dBm. Then S-parameters file was generated and in MultiMatch linear model was fitted to the S-parameters (Figures 8 and 9).

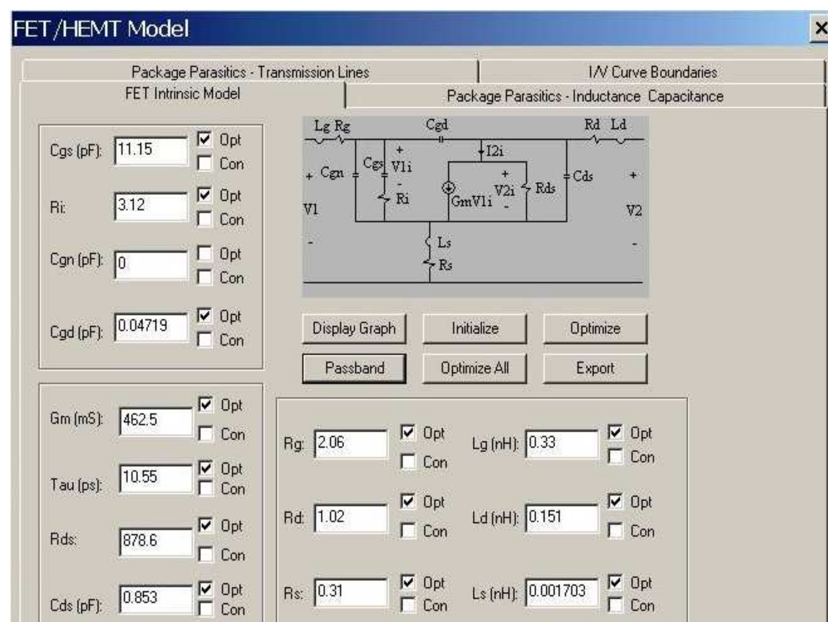

Figure 8. GaN HEMT linear model

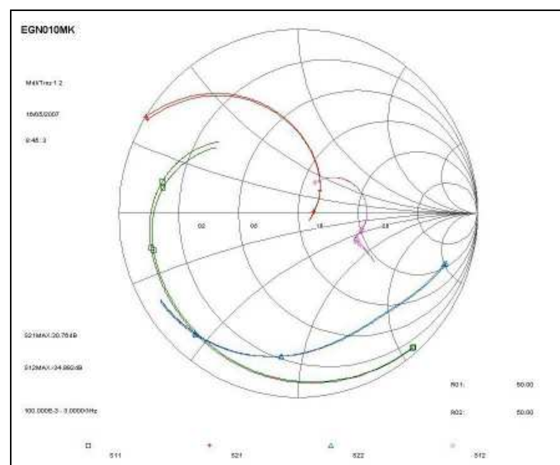

Figure 9. GaN HEMT *S-parameters* vs. linear model

The parasitic capacitances in the linear model have much smaller values than the GaAs MESFET ones and the parasitic drain-source resistor is much bigger. The optimum intrinsic load (across the voltage-current generator), RL_{opt}, of the GaN HEMT is about 100 Ohm while the GaAs MESFET one is about 4.5 Ohm (calculated by the Load-line method). All of this indicates that the GaN HEMT will have much wider bandwidth performance. The general capabilities analysis (Table 3) indicates that this transistor has much higher gain capabilities, but that comes at the price of substantial instability – the k-factor is bigger than one only between 3 and 4GHz. So the next step was to use the MultiMatch modification network synthesis capability to design a network at the input of the transistor that would, before everything, provide unconditional stability at all frequencies, but also would simultaneously level the gain, reduce the input miss-match and consequently widen the bandwidth and provide tolerance insensitivity of the performance of the stage. It should be obvious that such a network would contain resistors. With an initial guess about the bandwidth capabilities of the transistor of 1.6-2.3GHz such a modification network was synthesized and Figure 10 shows it in layout form.

FREQUENCY (GHz)	k -	MAG (dB)	MSG (dB)	Ga (dB)	Gw (dB)	GT (dB)
100.0000E-3	0.04	infinity	37.05	36.67	43.15	30.61
300.0000E-3	0.13	infinity	32.31	30.07	33.50	26.50
500.0000E-3	0.22	infinity	30.09	26.05	28.86	22.85
700.0000E-3	0.30	infinity	28.65	23.33	25.65	19.98
799.9999E-3	0.35	infinity	28.07	22.27	24.33	18.75
1.00000	0.44	infinity	27.14	20.52	22.04	16.62
1.20000	0.53	infinity	26.37	19.16	20.08	14.82
1.40000	0.62	infinity	25.71	18.07	18.36	13.29
1.60000	0.71	infinity	25.14	17.21	16.84	12.00
1.80000	0.79	infinity	24.60	16.53	15.48	10.92
2.00000	0.87	infinity	24.09	16.00	14.26	10.04
2.20000	0.94	infinity	23.59	15.61	13.16	9.33
2.40000	0.99	infinity	23.09	15.36	12.19	8.79
2.60000	1.03	21.49	21.49	15.22	11.32	8.41
2.80000	1.06	20.54	20.54	15.19	10.55	8.15
3.00000	1.08	19.81	19.81	15.26	9.88	8.02
3.20000	1.07	19.27	19.27	15.39	9.31	7.99
3.40000	1.07	18.79	18.79	15.54	8.83	8.00
3.60000	1.05	18.44	18.44	15.63	8.45	8.02
3.80000	1.03	18.20	18.20	15.55	8.16	7.99
4.00000	1.01	18.26	18.26	15.18	7.97	7.88
4.20000	0.98	infinity	18.14	14.45	7.90	7.65
4.40000	0.95	infinity	17.61	13.37	7.95	7.32
4.60000	0.92	infinity	17.08	12.05	8.12	6.94
4.80000	0.89	infinity	16.56	10.60	8.45	6.55
5.00000	0.86	infinity	16.06	9.12	8.96	6.15
5.20000	0.84	infinity	15.58	7.66	9.70	5.72
5.40000	0.81	infinity	15.11	6.26	10.72	5.15
5.50000	0.80	infinity	14.88	5.58	11.37	4.75

Table 3. GaN HEMT *k-factor* and Gain

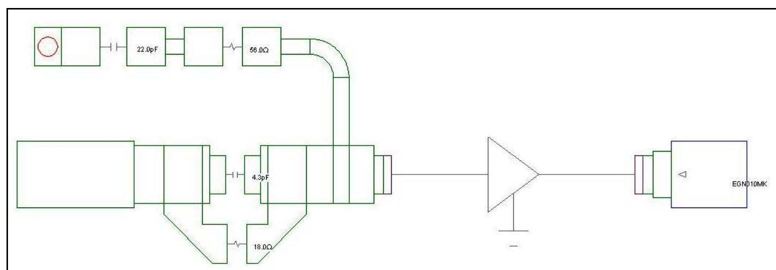

Figure 10. GaN HEMT modification network

Table 4 presents the results of the capabilities analysis, this time of the whole circuit of Figure 10. The optimum load (ZL_{opt}) for the maximum pre-clipped output power Po_{max}, Po_{max} itself and the associated maximum Gp_{max} are shown in the table.

DMS - STAGE ZL, Po and GAIN (PoM):

FREQUENCY (GHz)	LOAD TERMINATION (Ohm)		OUTPUT POWER (dBm)	POWER GAIN (dB)
1.60000	10.99	+j23.83	39.976	17.666
1.70000	10.48	+j23.07	39.981	18.441
1.80000	9.86	+j22.12	39.971	19.031
1.90000	8.91	+j20.31	39.969	19.370
2.00000	8.41	+j19.34	39.962	19.274
2.10000	7.98	+j18.48	39.952	18.877
2.20000	7.55	+j17.53	39.940	18.318
2.30000	7.17	+j16.60	39.929	17.693

Table 4. GaN HEMT ZL_{opt}, Po and Gp

Then the output network was synthesized by searching for a bandwidth in which Po would be no more than 0.5dB less than Po_{max} of Table 4. This was achieved for 1.7-2.2GHz which is also a very useful frequency range covering all the cell/mobile phone frequency bands. Figure 11 presents the GaN HEMT Load-Pull contours for the 1.7-2.2GHz bandwidth. The blue line again was the targeted by the synthesis $ZL_{opt.}$

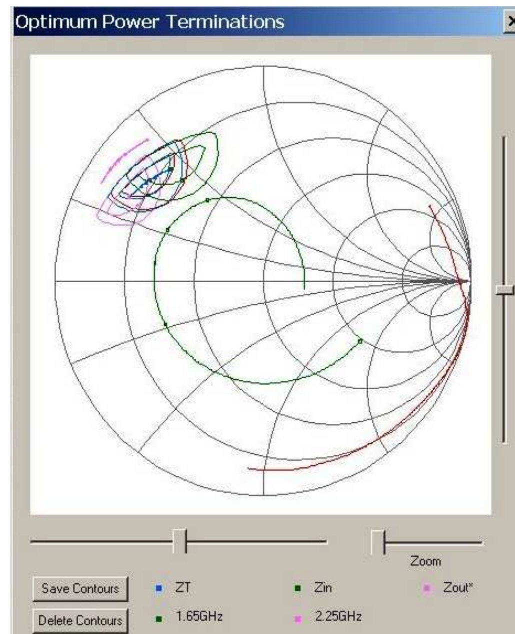

Figure 11. GaN HEMT Load-Pull contours for P1dB

Figure 12 presents the Gp and the input and output RL after the input matching network was added. Figure 13 shows the layout in MultiMatch and Figure 14 shows it after it was transferred into Microwave Office. As it can be seen, the series microstrip lines have much higher characteristic impedances, which reflects the much higher transistor impedances and the wider bandwidth that can be achieved compared to the GaAs MESFET case.

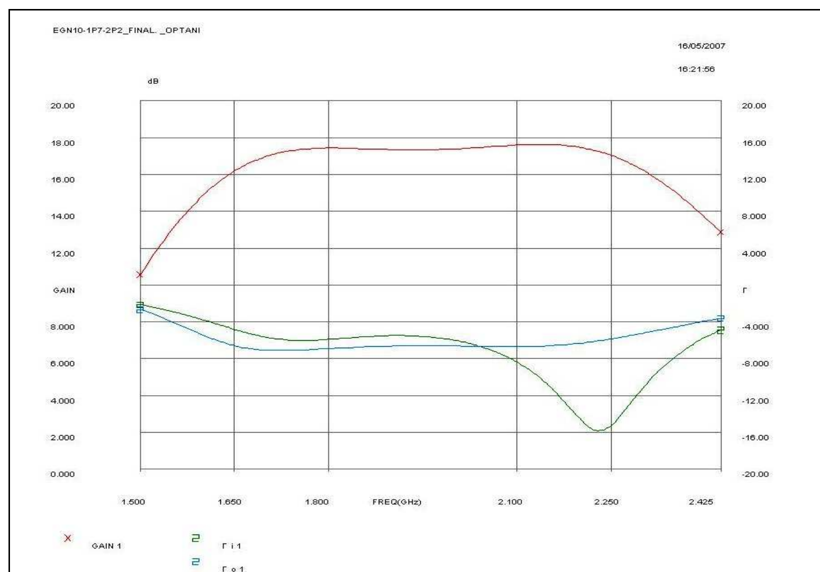

Figure 12. GaN HEMT Gp and RL

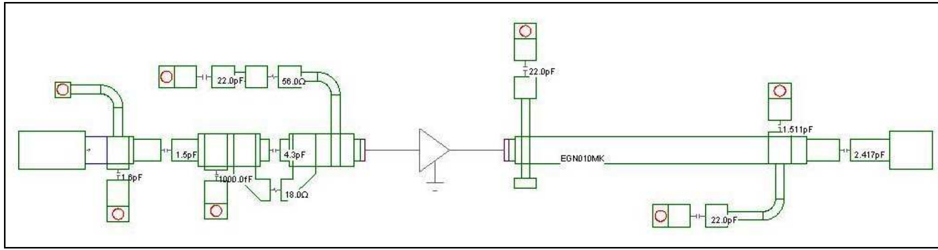

Figure13. GaN HEMT stage MM layout

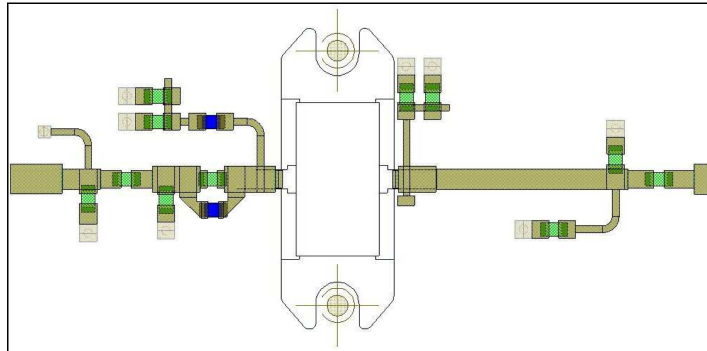

Figure 14. GaN HEMT stage MWO layout

The circuit in Microwave Office was very slightly tuned and it simulated P1dB of better than 40.2dB over the 1.7-2.2GHz bandwidth (Figure 15). The simulation for Figure 15 was done by copying the equations and the script file from the Microwave Office example project "P1dB_User_Defined_Measurement.emp". Figure 16 compares the Gp and RL between the simulated and the measured performance of the first two test units that were built. No tuning was applied to the test units.

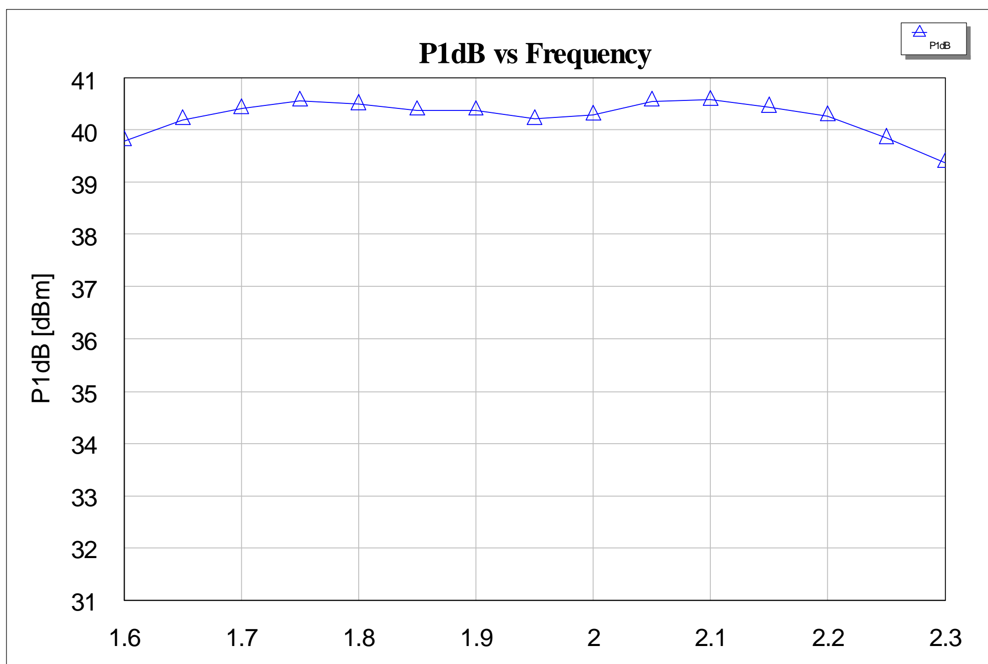

Figure 15. GaN HEMT stage MWO simulated P1dB

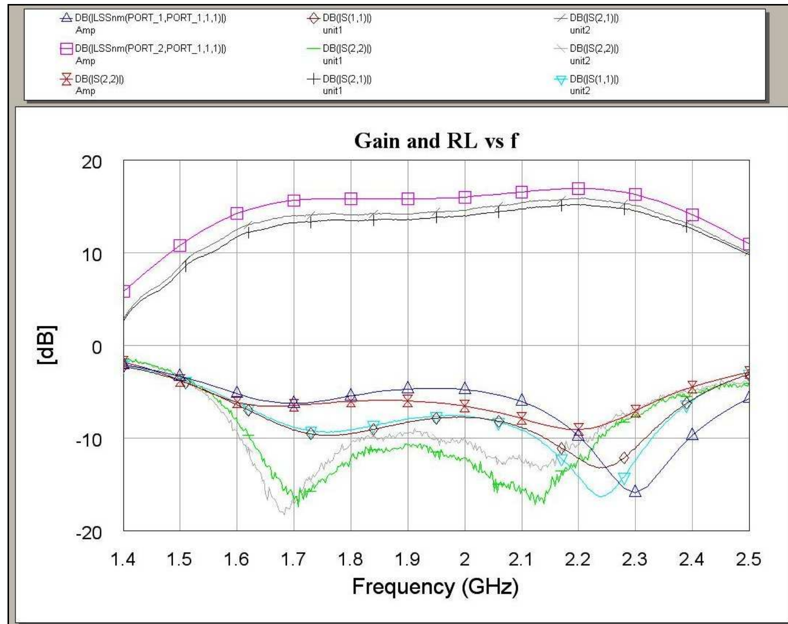

Figure 16. GaN HEMT stage simulated and measured Gp and RL

The simulated gain is about 1.5dB higher that the measured values but with the same shape. It was even 2dB higher before the operational temperature in the nonlinear model was adjusted up by a whole 30°C to counter for the non-perfect heat-sinking of the test units. Also the measured output IP3 in this case is 49.5dBm while the simulated output IP3 of 58dBm is overly optimistic. It is difficult to establish the reason for these differences without more data.

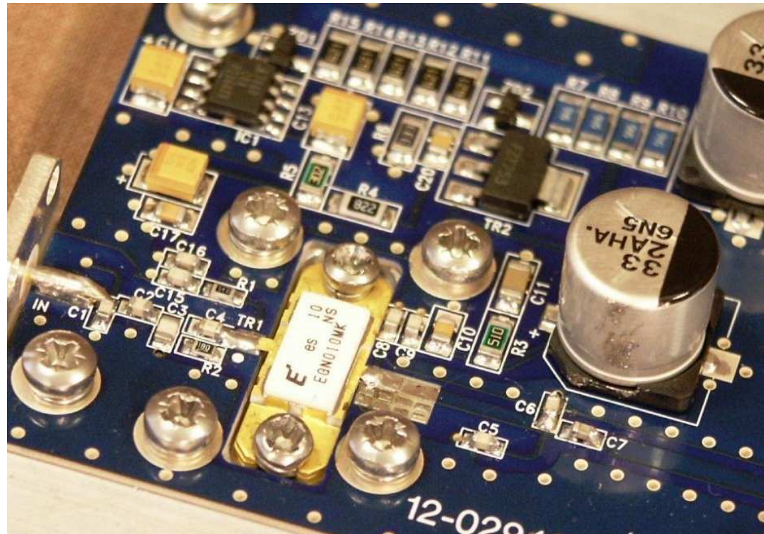

Figure 17. GaN HEMT test unit photo

What is important though is that the measured P1dB of both units again came charmingly on top of the simulated P1dB. So as a whole, the combination of the nonlinear model and the design approach provided in effect a first-time-right design. Figure 17 shows a photograph of one of the GaN HEMT test units. The GaAs MESFET test units look very similar.

Summary and Conclusions

As expected the GaN HEMT showed much broader bandwidth and higher gain capabilities. The GaAS MESFET though showed exceptionally good linearity. It is as if it has a linearizer integrated in its structure. The relatively poor linearity performance of the GaN HEMT in a Class A amplifier realization is not necessarily a bad thing. The non-impressive third-order distortion levels could

possibly correspond to a gradual gain compression curve which together with the much lower parasitics would allow for very good and easy to achieve pre-distortion type linearization. The lower parasitics are really of great advantage when the GaN HEMTs are used in the heavy nonlinear switch-mode amplifier applications (E, D, F) and for envelope biased Class AB applications, both of which are providing exceptional efficiency. The latter ones are also easily linearized by digital pre-distortion. There are already numerous technical and scientific publications on these matters. There is a great excitement in the industry about utilizing the advantages the wide bandgap transistors are offering. Mass product applications are coming, competition is boiling up and hopefully the current high cost of the GaN transistors will come down soon.

The GaAs MESFET nonlinear model used is very good. The GaN HEMT model is good enough for this application. With the SiC and GaN microwave transistors that have come recently on the market most of the transistor manufacturers are finally warming up to the necessity of providing good and really usable nonlinear models. There are also companies like Modelithics and Auriga Measurement Systems that provide modeling services.

Once again as in [2] and [3] it was shown that the dedicated to amplifier design MultiMatch with its unique Power Parameters and practical real life network synthesis capabilities guarantees first-time-right and optimum performance designs in very short design cycles. It should be emphasized though that MultiMatch is really effective if the users have a thorough understanding of amplifier and matching network basics and are determined to develop superior products. It is not a design tool for Dummies! Actually even for experienced amplifier designers MultiMatch, with its unique amplifier synthesis design approach, will provide insights and solutions which are impossible when using just a general simulator/optimizer type software programs. At the same time the software also provides a path for inexperienced users with good fundamental knowledge to learn and realize quickly practical and effective amplifier designs.

Microwave Office was an integral part of the design procedures described here. As a general RF/microwave simulator it is very user-friendly and with its open design environment it provides easy interoperability with third-party design tools. As one of the very broad range of interconnected RF/microwave electronic design automation products of AWR its solutions can be integrated and used further in the simulations for the development of more complex systems.

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8. Microwave Office is a registered trademark of Applied Wave Research, Inc.