A 10 bit 2.2Gsps ADC Operating Over First and Second Nyquist Zones

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Abstract:

This paper introduces a 10 bit 2.2 Gsps (Giga sample per second) fully bipolar Analog to Digital Converter, developed on a 75GHz cut off frequency HBT SiGe process, designed for operation over first and second Nyquist zones. Performances over 8 effective bits have been demonstrated up to 2 Gsps Nyquist.

1. Introduction

A high speed ADC that offers good linearity over a range of high frequency inputs is a key component for tomorrow's broadband RF transmitters using high Intermediate Frequency (IF) architectures.
New architectures for ADC allow now to reach performances which were barely conceivable a few years ago. Broadband IF Sampling ADC architectures are today capable of directly digitizing wideband signals around second or first IF zones while keeping excellent linearity performance, paving the way to Software Radio. The architectural shift to broadband data conversion leads to increased ADC sampling rate thus creating new challenges in design, package and test methodology.
A 10 bit 2.2 Gsps ADC has been developed based on a 75 GHz SiGe HBT process, including special features for better industrial test coverage.
Key issues for design, test and circuit specification, altogether with characterization results are presented and analyzed.

2. Purpose of high speed ADCs

An ADC is used to produce a quantization of a continuous time varying continuous signal, therefore part of the information included in the input signal will be lost by this sampling and quantization process (aliasing, quantization noise), and some parasitic information will be added due to the non ideality of the ADC (aperture uncertainty, thermal noise, non linearity).
The relevance of an ADC for a given application is its ability to keep the ratio of useful information over parasitic (or undesired) information as high as possible for a given power budget.

A good ADC must be able to code a small signal close to a large signal (interferer). This feature is mandatory for any broadband (multi channel) application were an ADC is used to code all the channels and the demodulation is performed through digital processing. The constraint on the ADC is thus on inter-modulation products (IMD) which level must be below the smallest signal to code.

2.1 Relevant parameter for ADC specification

Global parameters such as Effective Number Of Bits (ENOB) are not always relevant to select the best possible ADC for a given application. This is especially true for very high speed ADC (over 1Gsps), because of the very large bandwidth of integration, Signal to Noise Ratio is dominated by thermal noise, and SNR becomes the dominant factor in ENOB. Therefore ADC displaying similar ENOB figures may have very different linearity figures (Spurious Free Dynamic Range and/or Total Harmonic Distortion). For instance an ADC featuring 8 bit ENOB can display only 50dB SFDR while another would display 60dB SFDR.
Furthermore, frequency independent and deterministic non ideal characteristics of the ADC can be compensated by digital signal processing (e.g. look-up table).
For operation at Nyquist (Fin~Fs/2) and above, the clock phase noise (also called jitter) has direct impact on SNR. Jitter can be split in 2 components: external jitter (due to the sources used, or potential board routing issues), and internal jitter (generated in the ADC by thermal noise on clock path, coupling with other signals, or poor power supply rejection). Therefore internal jitter is also a very important parameter of the ADC.
Parameters to consider for a high speed ADC are therefore: THD, SFDR, IMD (multitone), SNR, Noise Power Ratio (for broadband application), ADC added Jitter (for 2nd Nyquist application).

2.2 Parameters for comparison of ADCs

An SNR value is relevant only if considering also the ADC sampling frequency altogether with the ADC full scale, combining the three informations we can produce a relevant indicator of ADC performance, the per Hz Normalized Noise Floor expressed in dB_m/Hz :

$$NNF = FS[dBm] - SNR[dB_{FS}] - 10*\log(Fclock/2)$$

Reachable limit of NNF for a reasonable power dissipation seems to be about $-150dB_m/Hz$.

Another relevant indicator of ADC performance is the quantization energy, that is the energy needed to deliver an "effective" level of quantization:

$$E_Q = P/(F_{sampling} * 2^{ENOB})$$

where P is the ADC power dissipation.
E_Q should of course be kept as low as possible.
Normalized Useful Bandwidth can be defined as: NUB=Finmax/Fclock (where Finmax is maximum input frequency leading to a 3dB degradation of SINAD).
These indicators allow for comparisons between ADC designed for various domains of operation.

3. Design challenges

As previously discussed a pertinent 10 bit high speed ADC should meet the following criteria:

1. Linearity over first and second Nyquist zone : beyond 57dB SFDR.
2. Good NNF: around or below -145dB$_m$/Hz
3. Stable spectral response over sampling rate, temperature and input frequency to allows for single look-up table processing.
4. Clock phase noise added by the ADC must be kept as low as possible.
5. Power dissipated and E_Q must be as low as possible.
6. Bit Error Rate should be kept at a level compatible with the application (values commonly admitted : instrumentation 10^{-12}, transmission 10^{-6}).

Items 1/ and 2/ are related to the internal front end Track and Hold (T/H) which is mandatory for Nyquist and above Nyquist operations, and T/H clock management in the ADC, item 3/ is related to settling through the quantifier. Item 4/ is related to the clock tree design strategy. Item 5/ is related to the overall design strategy of the ADC, and item 6/ is depending on the decoding and logic part of the ADC.
When taking all these factors into consideration two architectures are possible:

1. A single core ADC
2. A massively interleaved ADC [1]

We have discarded this second option because of clock jitter management issues. Nevertheless our ADC features all the tuning needed to allow for easy interleaving (offset adjust, gain adjust, aperture delay fine adjust).

3.1 Front End Track and Hold Amplifier

In a fast ADC the front end T/H is a major design issue. The performances of the ADC will be dominated by the performances of the front end T/H, granted that the quantifier settles properly in its time slot. Depending on the front end T/H, the ADC will be able to operate over first and second Nyquist zones, over first Nyquist zone only or in base band only.
Most of the thermal noise is also generated in the T/H and associated preamplifiers, so special care must be taken in the trade-off of power and noise.
The structure retained for the T/H stage was based on a fully differential S.E.F (Switched Emitter Follower), since this structure is well known for its robustness. A differential output amplifier is used to filter out the common mode bounces at the T/H output before driving the analog quantifier. A gain 2 differential input amplifier, featuring offset adjust, is used in front of the T/H in order to be able to display a constant impedance at the ADC input thus allowing analog filtering.
The main difficulty is to keep a good linearity over the second Nyquist zone, since in this frequency domain closed loop structures are not relevant. We will see in the result section that performances are quite good.

3.2 Quantifier

Quantifier structure choice is a key issue in the design of an ADC, specially when we are looking simultaneously for speed, accuracy and power efficiency.
Pipeline and sub-ranging architectures are discarded, because for this sampling range they are not relevant, especially regarding B.E.R (Bit Error Rate) issue.
A full flash architecture is also not acceptable because of loading effect caused at T/H output due to too many comparators (2^{10}+1), and also because of power spillage that this architecture would imply.
Finally we retained a successively folded and interpolated architecture which offers the best trade-off between speed, accuracy and power dissipation.
The MSBs are generated by a coarse cycle pointer, and are corrected in accordance with LSB's transition in the logic part. Gain adjustment is made by controlling the bias of the reference resistor chain.

3.3 Logic part

The function of the logic part in a fast ADC is three fold:

1. Provide a B.E.R. compatible with the specified application (e.g: 10^{-12} for instrumentation).
2. Realize the fusion between MSBs and LSBs delivered by the quantifier, and eventually correction of MSBs.
3. Convert the internal coding into Binary code.

3.3.1 Bit Error Rate

The purpose of regeneration latches is to convert analog signals coming from the quantifier into full swing synchronized logical signals for further processing.
When an analog level coming from the quantifier is very close to its transition level the regeneration latch will perform one of the following:

1. Take the good decision and produce a full swing logical level.
2. Take the wrong decision, and produce a full swing logical level, depending on the internal coding the impact can be major (Binary coding, glitch energy 2^N quantum, where N is the index of the considered bit), or minor (Gray coding, glitch energy 1 quantum, because only one bit can be in the danger area at a time).
3. Take no decision (i.e. meta-stability), or produce a logic level of reduced swing which jeopardize subsequent logical operation.

Taking no decision causes B.E.R. In this case the latch does not have enough time to generate a true logical

level from analog signal coming from the quantifier, thus jamming the subsequent decoding.
With an increase in the sampling rate, B.E.R is a major issue which cannot be neglected. To minimize B.E.R. it is necessary to use latches which have very low divergence time constant, and/or to spread the divergence over several half clock period.

3.3.2 Merging of MSBs and LSBs

The second function of the logic part is to combine information coming from the MSB (coarse) and LSB (fine) sections, in order to produce a full length word. This function performs a correction of the coarse (inaccurate) transitions in accordance with the fine (accurate) transitions. We have been using this method successfully for many years beginning with TS8388 [2] (8 bit 1 Gsps ADC), released in 1997.
The NRZ function is also performed in this logic block. This function makes sure that underflow (or overflow respectively) will not produce codes other than the minimum code (or maximum code respectively).

3.3.3 Binary encoding

The code conversion from Gray code to natural Binary code is rather straightforward: a cascaded XOR from MSB to LSB. To avoid limitations due to propagation ripple in this decoding, we have spread the decoding over one and a half clock periods. This decoding circuit includes a multiplexer, in order to be able to deliver also Gray code at the output of the ADC.
The output of this decoder is feeding a master slave bank of latches driving differential ECL / LVDS compatible output buffers.

3.4 Clock tree

For a fast ADC operating in second Nyquist zone, the jitter observed on the switch of the T/H amplifier can dramatically degrade the performances in term of SNR.
Special care has been taken in the design of:

- the clock circuitry in order to minimize the jitter induced on chip,
- the package which was optimized to avoid coupling between the clock and other "unclean" signals, altogether with thermal management optimization [3].

The first idea is to use a fully differential circuitry in order to have optimal rejection of power supply ripple, and to induce as little as possible power supply ripples.
The second idea is to use internal clock edges as steep as possible in order to minimize the thermal noise effect at each stage of the clock path. For the same reason the clock driving the T/H switch must be kept as sharp as possible.
There is a direct relationship between internal clock edge sharpness, fastest transient (or maximum signal frequency) to digitize and acceptable thermal noise level in clock circuitry to meet a specified SNR level.
All the structures used in the clock tree have already been proven in our former 10 bit 2Gsps ADC TS83102G0 [4]. The measured jitter including board, generator and ADC, based on locked histogram method, using very good generators is about $150fs_{rms}$.
A test mode provides special clocking for output latches, decimating by 32 the converted data, thus delivering a word rate compatible with industrial test.

4. ADC main features

This ADC is now introduced as a standard product referenced AT84AS008 [5], it is mechanical and electrical compatible with TS83102G0, but offers extended performances and extended functionality domain while saving 10% of power, thus allowing seamless upgrade of system designed with TS83102G0.

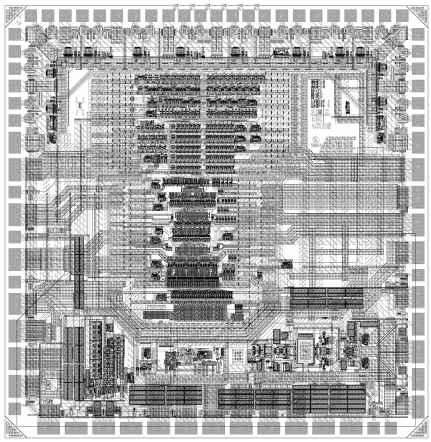

Figure 1: View of the ADC layout

Die size :14.7mm2
Process: SiGe HBT 75GHz cutoff , 3 layers of metal
Max Sampling Rate: 2.2Gsps
Full Power Input Bandwidth: 3.5GHz
Full Scale: 500mVpp diff (tunable +/-10%).
Power dissipation : 4.2W
Package: CBGA152, pitch 1.27mm.

5. Characterization results

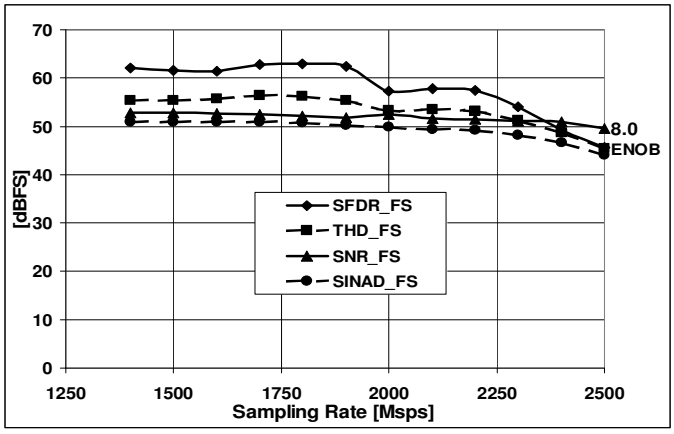

Figure 2: SFDR, THD, SNR, SINAD vs Fclock at Nyquist , Ain=-1dB_{FS}

Test characterization has demonstrated very good operation over first (figures 2, 5) and second (figure 3) Nyquist zones up to 2.2Gsps, ENOB at Nyquist is over 8.0 bits up to 2Gsps.

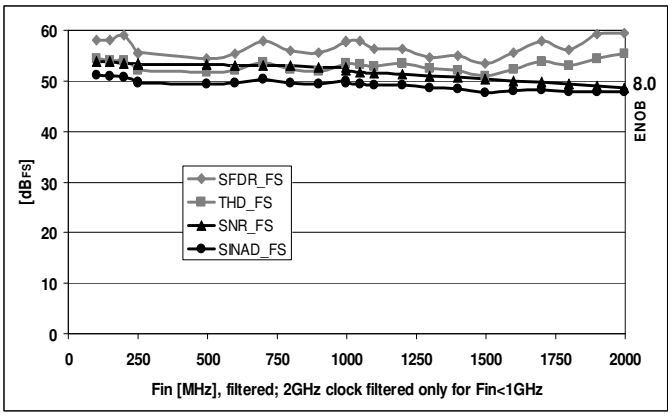

Figure 3: SFDR, THD, SNR, SINAD vs Fin at Fclock=2Gsps, Ain=-1dB$_{FS}$

Characterizations demonstrated also a good performance stability over a wide temperature range (figure 4).

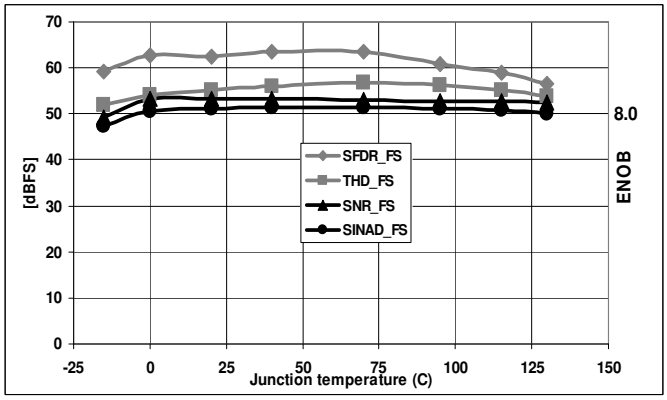

Figure 4: SFDR, THD, SNR, SINAD vs Tj at 1.7Gsps, Fin=848MHz, Ain=-1dB$_{FS}$

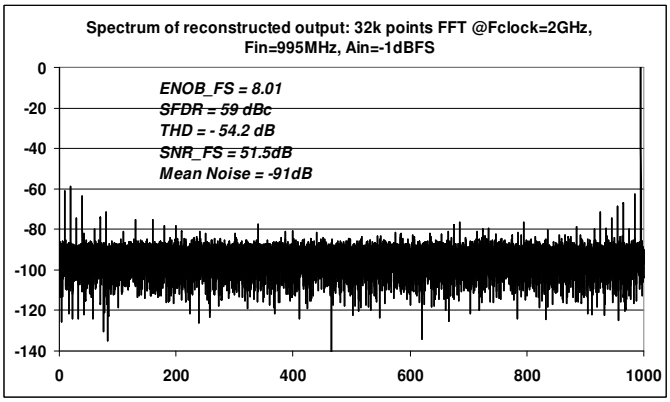

Figure 5: 32k points FTT spectrum at 2Gsps, 995MHz, Ain=-1dB$_{FS}$

6. Conclusion

We have designed a fast ADC for Nyquist and above Nyquist operation, exhibiting a unique Normalized Noise Floor (NNF) while keeping a Quantization Energy (E_Q) among the lowest in its frequency range. Furthermore, we have pushed the sampling rate beyond 2 Gsps while keeping an ENOB of 8.0 bits at Nyquist, and offering outstanding performance over second Nyquist zone, thus paving the way to high intermediate frequency (IF) digital processing.

7. Acknowledgements

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References:

[1] Ken Poulton, et al "A 20GS/s 8b ADC with 1MB Memory in 0.18µm CMOS" ISSCC Digest of Technical Papers, Feb 2003.

[2] Datasheet of e2v's TS8388B 8 bit 1Gsps ADC, rev 2144C-BDC-04/03.

[3] Benoit Dervaux, "A Ceramic BGA 148 Package for assembly of a 2 Gsps Analog to Digital Converter", *European Microelectronics Packaging and Interconnection Symposium, Cracow, Poland, 16-18 June 2002.*

[4] Datasheet of e2v's TS83102G0B 10 bit 2 Gsps ADC rev 2101D- BDC-06/04.

[5] Summary datasheet of e2v's AT84AS008 10 bit 2.2Gsps ADC, rev 5404AS-BDC-01/05.