An Investigation into the Effects of Sampling on the Loop Response and Phase Noise in Phase Locked Loops

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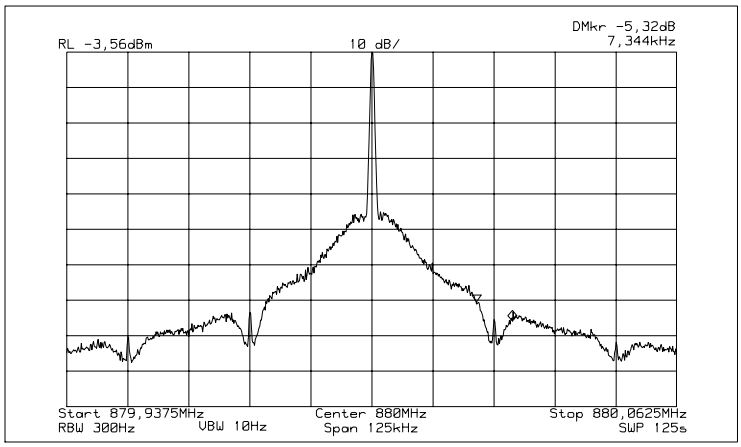
Abstract. The majority of Phase Locked Loop (PLL) IC manufacturers provide simulation software to enable the performance of their ICs to be evaluated. These simulation packages use a continuous time model to calculate the loop response and predict phase noise performance. When the loop bandwidth is relatively large compared to the comparison frequency this model becomes less accurate and the effect of sampling must be taken into account. This paper compares the results of the continuous time model and the sampled model and introduces a base-band circuit that simplifies the process of making measurements to support the simulations and provide further insight into the effects of sampling.

Introduction

Most who have worked on PLL based synthesisers have at one time or another seen a display where there are significant nulls in the noise at the comparison frequency offset and its harmonics as in Figure 1.

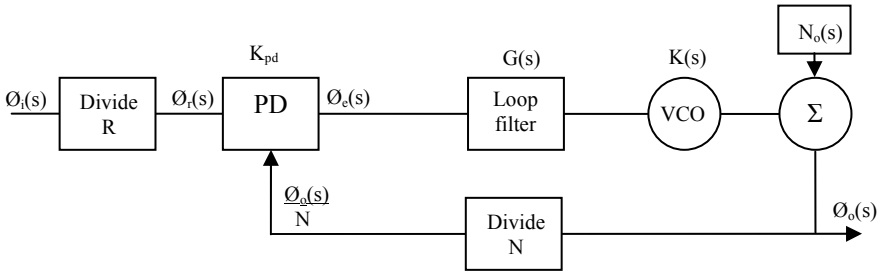
Figure 1



However the evaluation software provided by the PLL manufacturers [1] ignores these effects which may lead to errors in the system calculations. This effect is mentioned in some books and attributed to sampling but no further explanation is offered [2]. The mathematics to analyse these effects has been developed in [3]. The resulting equations are used to illustrate the difference between the continuous time and sampled models, and measurement results presented to verify the calculations. Measurements at radio frequencies can be complex and time consuming and often require expensive equipment so a base-band circuit is introduced that emulates the PLL and provides a useful platform for investigating some properties of PLLs. The circuit enables measurements to be made at low frequencies and different configurations to be investigated without the difficulty of design at radio frequencies.

1. PLL continuous time model

Block diagram of continuous time PLL model.



The open loop gain is given by:

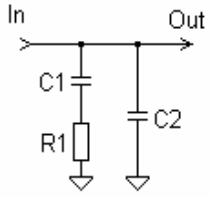
$$G_{OL} = \frac{GK(s)}{N} \qquad (1)$$

And the closed loop transfer response is given by:

$$Tr(s) = \frac{GK(s)}{1 + \frac{GK(s)}{N}} \qquad (2)$$

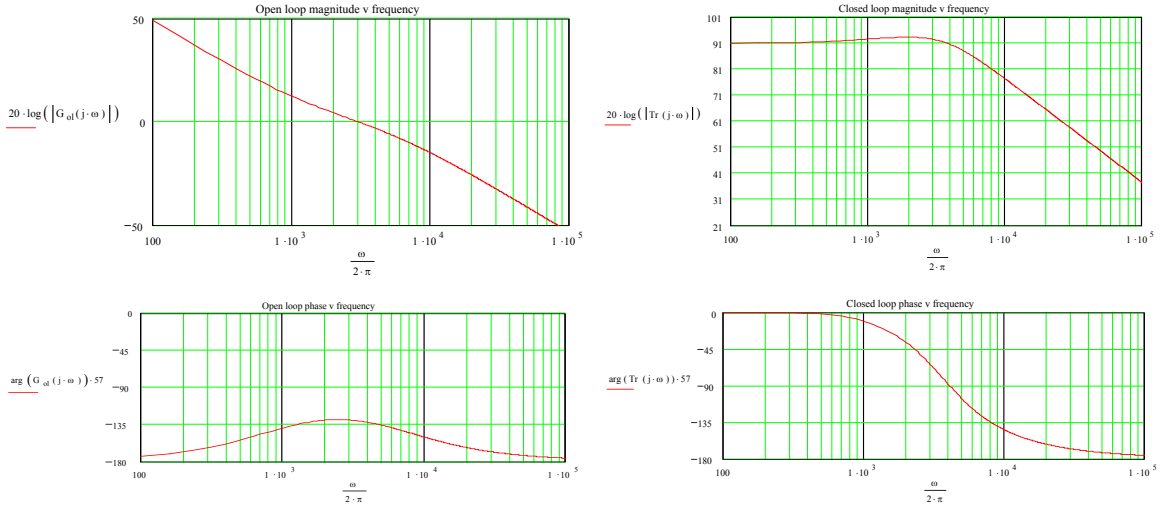
Where $GK(s) = G(s) \cdot K(s)$ and $K_{pd} = 1$

The phase detector is of the charge pump type and the loop filter used is of the standard lead lag form.



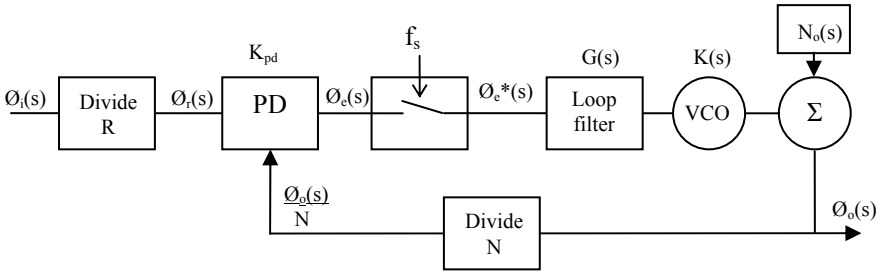
The simulation plots below (Figure 2) show the familiar open loop and closed loop frequency and phase response of the linear continuous time model

Figure 2



2. Discrete time sampled PLL model

Block diagram of sampled PLL model.



Where $Ø_e^*(s)$ indicates the sampled version of $Ø_e(s)$.

The open loop gain for the sampled loop is given by:

$$G_{OL}^*(s, f_s) = \frac{1}{N} \cdot \sum_{n=-10}^{10} GK(s - j \cdot n \cdot 2 \cdot \pi \cdot f_s) \qquad (3)$$

The summation should theoretically be from -∞ to ∞ but using -10 to 10 provides sufficient information for the purpose of this investigation and cuts down on computation time for simulations.

Figure 3 shows the calculated open loop gain using equation (3), and Figure 4 shows the measurement of the open loop gain made on the test PLL. In contrast to the continuous time model the loop gain is aliased around each harmonic of the sampling frequency.

Figure 3

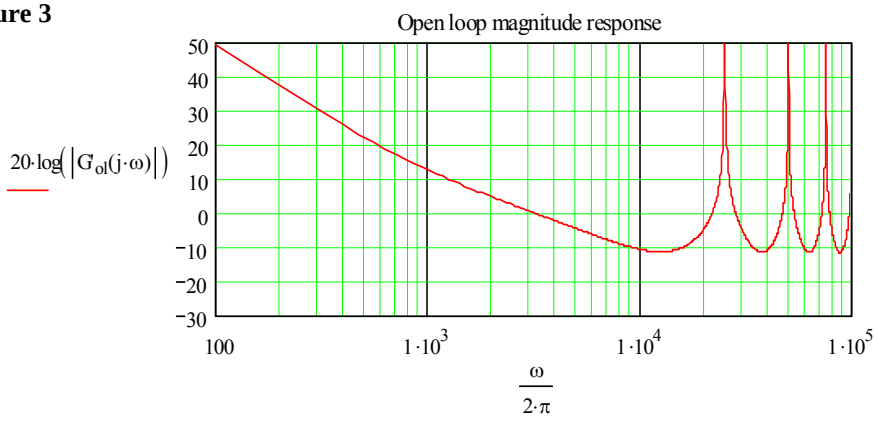
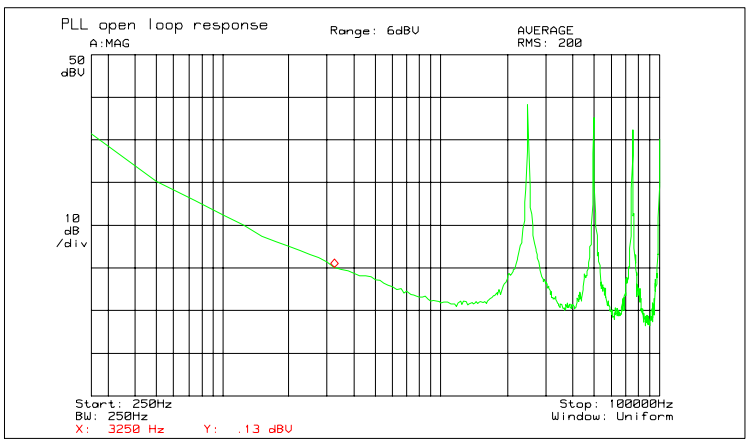


Figure 4



The closed loop transfer function for the sampled loop is given by

$$Tr^*(s, f_s) = \frac{GK(s)}{1 + \frac{1}{N} \cdot \sum_{n=-10}^{10} GK(s - j \cdot n \cdot 2 \cdot \pi \cdot f_s)} \qquad (4)$$

Figure 5 shows the calculated closed loop transfer function, and Figure 6 shows the measurement made on the test PLL. Both simulation and measurement show the response goes to zero at multiples of the sampling frequency.

Figure 5

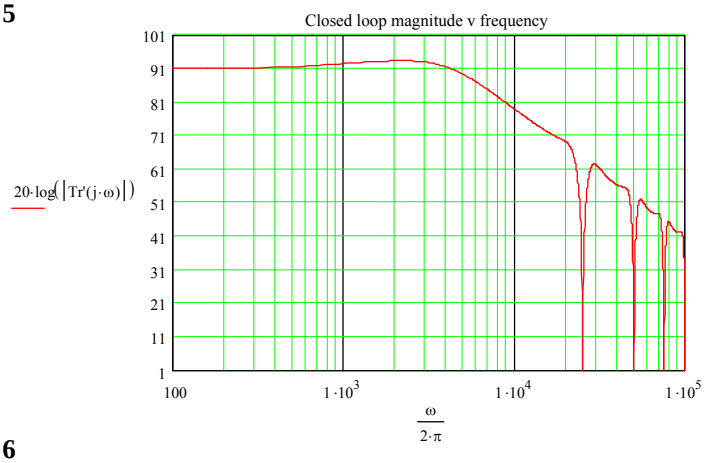
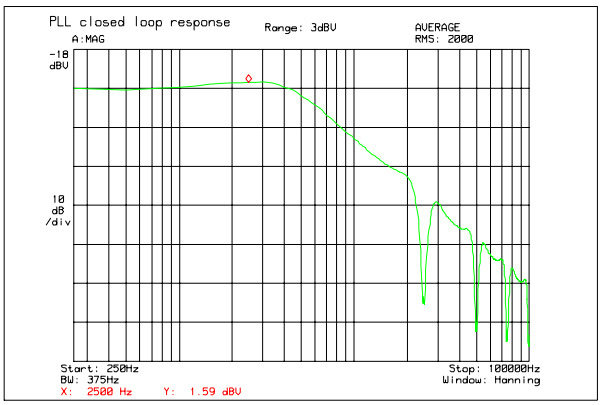
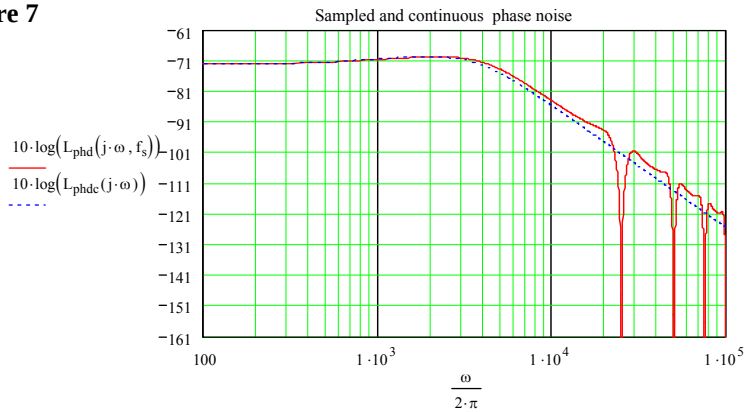


Figure 6



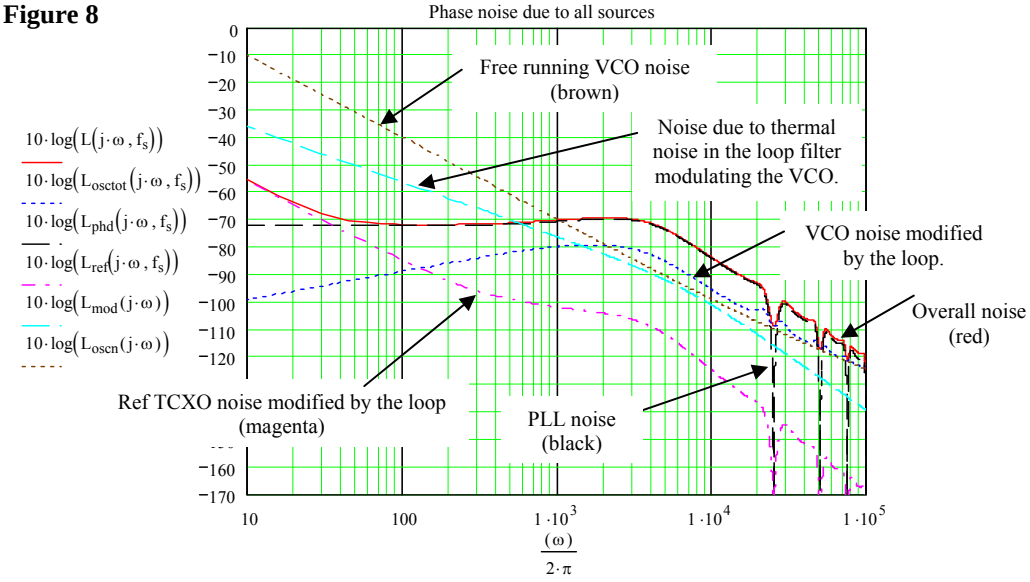
A simulation of the continuous time and sampled loop transfer functions (Figure 7) shows the difference between the two. It can be seen that the sampled model differs significantly from the linear model and predicts a wider bandwidth and nulls in the response that occur at the comparison frequency and its harmonics.

Figure 7



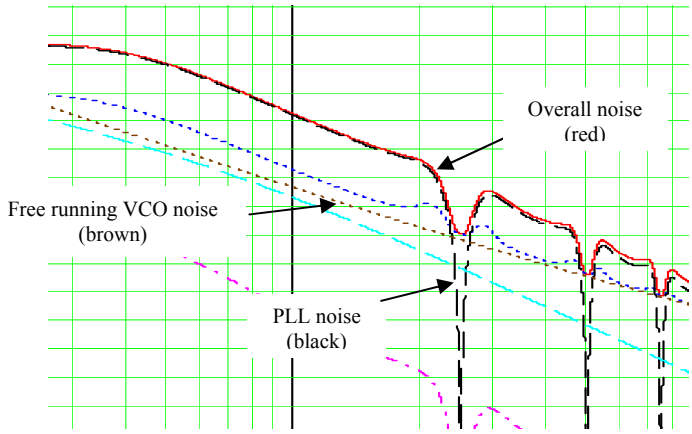
Noise sources such as reference noise, phase detector noise, Voltage Controlled Oscillator (VCO) noise and thermal noise in the loop filter can be added to the simulation and the contribution from each, and the overall noise, can be plotted (Figure 8).

Figure 8



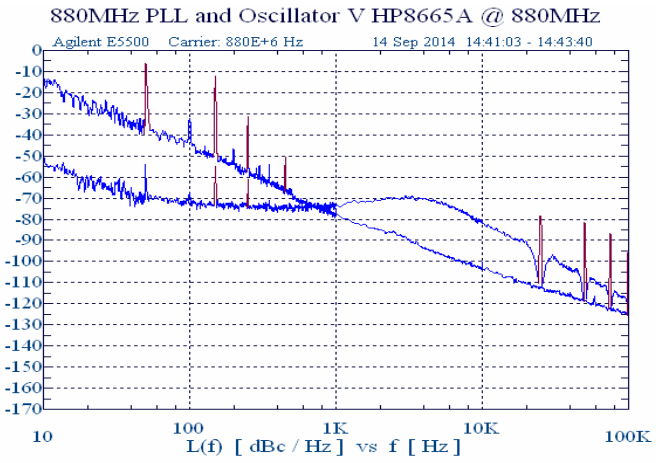
Taking a closer look at the nulls at it can be seen that the phase noise closely approaches the level of the free running VCO noise (Figure 9).

Figure 9



Finally a phase noise measurement on the test PLL and the free running VCO confirms that the simulation is quite a good match to the real thing (Figure 10).

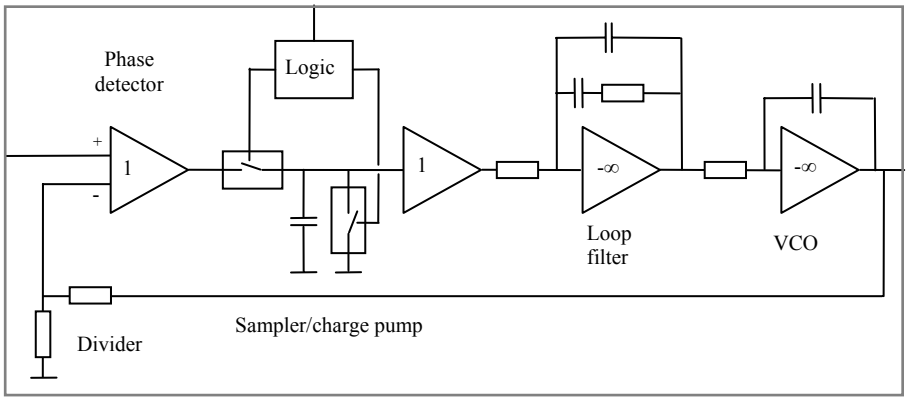
Figure 10



3. Reconstructing the PLL at base-band

Most simulations, and the calculations used above, reduce the loop components to their base-band equivalent. By making the substitution of voltage for phase and using a few simple blocks we can produce some hardware at base-band that replicates the action of the PLL. The advantage of using this circuit to simulate a PLL is that it allows parameters such as comparison frequency, loop gain and VCO gain to be adjusted by simple components changes rather than having to consider the design a whole range of oscillators, and performing complex measurements at radio frequencies.

Block diagram of PLL emulator.



Phase detector: The phase detector gives us the difference in phase between two signals fed to its inputs. In the baseband circuit a differential amplifier gives us the difference between two voltages.

Sampler/charge pump: The sampler converts the output from the phase detector into narrow voltage pulses with a magnitude representing the output from the differential amplifier (phase detector) which are buffered by the unity gain amplifier. The sample control circuit provides a short pulse to the series switch which transfers the voltage to a hold capacitor. The value is held for $1/10^{th}$ of a sampling cycle then clamped to zero by the shunt switch. Although this is not a perfect impulse sampler it turns out to be good enough. Since the input to the loop filter amplifier is a virtual earth the voltage pulses are converted to current pulses by the resistor between the buffer and the loop filter amplifier. There is a slight difference in operation compared to the PLL in that the PLL generates fixed value currents for a variable time whereas this circuit generates variable value currents of a for a fixed time but ultimately they both produce charge packets of the same magnitude.

Loop filter: The loop filter takes current pulses (charge packets) from the sampler/charge pump and converts them to an output voltage in the same way as the loop filter in a PLL takes the current pulses (charge packets) and converts them to a voltage for the VCO.

VCO: In the PLL the oscillator acts as an integrator of phase and has units of radians/second/volt. In the base-band circuit this is replaced by an integrator that generates an output in volts/second/volt. The equivalent VCO gain is set by the R and C values.

Divider: In the PLL the divider divides the phase by the division ratio of the divider. In the base-band circuit where voltage has been substituted for phase the divider is implemented with a simple voltage divider.

4. Sampled signals

The sampler section is isolated from the rest of the circuit to make some simple measurements.

Block diagram of sampler set-up.

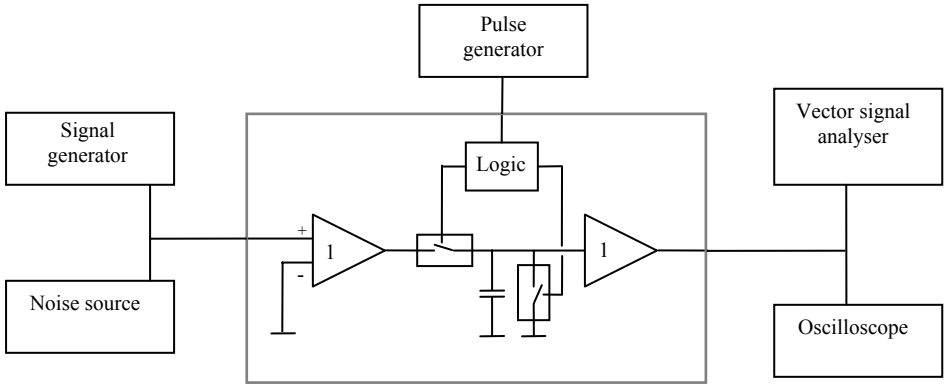


Figure 11 shows a sine wave being sampled by the sampler circuit. A hold time of $1/10^{th}$ of the sample period is used as a good compromise for approximating an impulse sampler without introducing problems with gain and delay. (The gain of the sampler is $1/10^{th}$ and the delay is ½ of the pulse width). The noise source is switched off for this measurement.

Figure 11

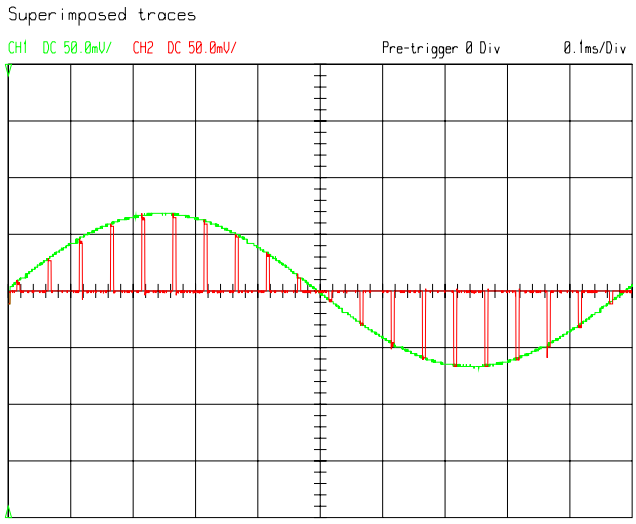
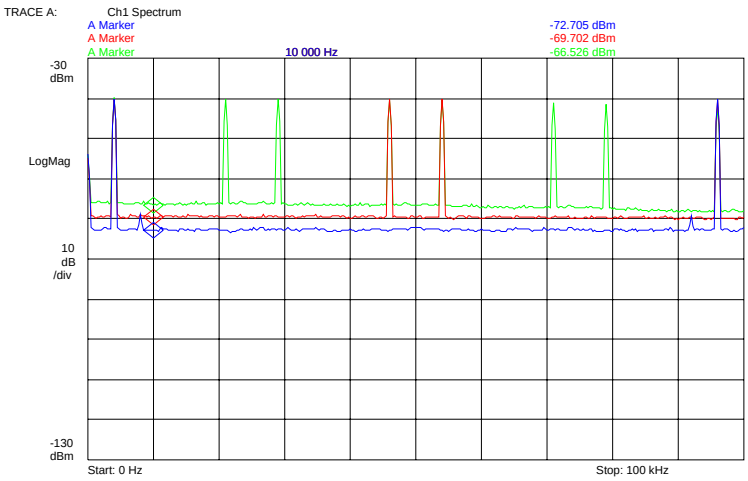


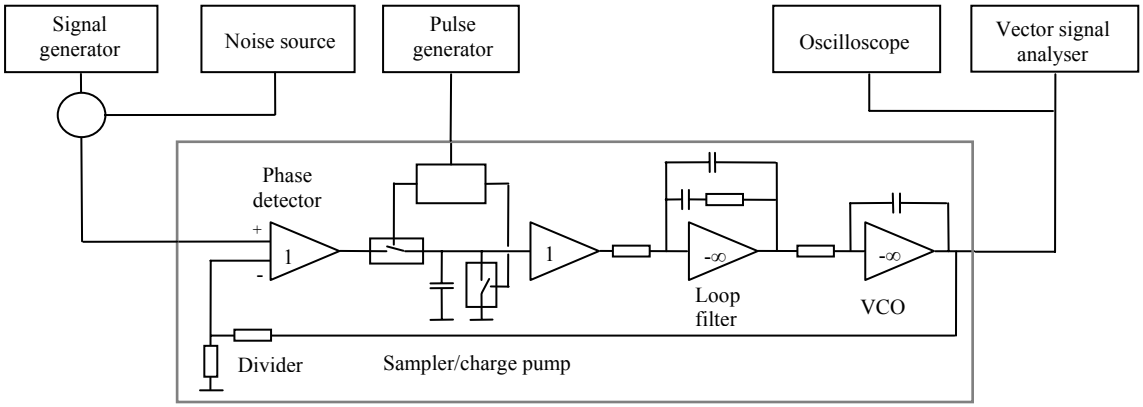
Figure 12 shows the effect of sampling in the frequency domain. A 4kHz sine signal is summed with broadband noise to observe the effect of the sampling frequency on each. The sampling frequency is set to 25kHz, 50kHz and 100kHz. As we would expect we see images of the 4kHz sinusoid about each of the harmonics of the sampling frequency. We also observe, as we would expect from sampling theory, the noise density falls by ~3dB every time we double the sampling frequency.

Figure 12



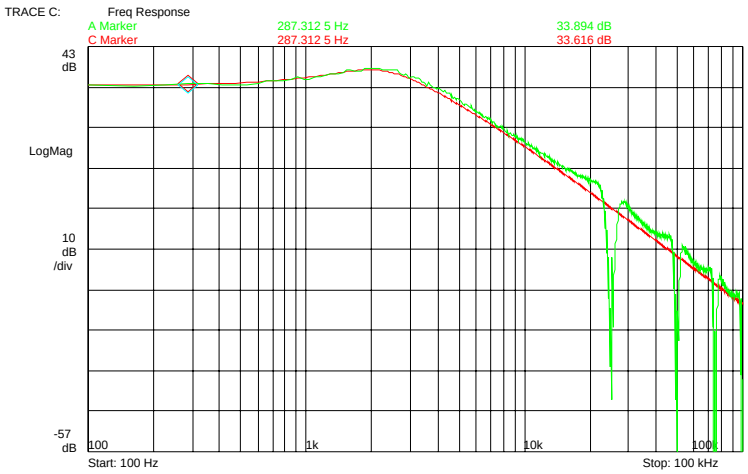
5. Closing the loop

The complete loop is now connected as shown in the diagram below.



The sampler is first disabled by setting the series switch permanently on and the shunt switch off to create a continuous time model and the signal generator turned off so that the response may be measured using broadband noise as the input. The measurement is accomplished by taking many averages at the output. The more averages the smoother the trace.
The sampler is then enabled and the gain adjusted for the sampling pulse width and a measurement is taken in the same way as before. Figure 13 shows the two responses plotted together and confirms the difference in loop response predicted by the calculations (Figure 7).

Figure 13

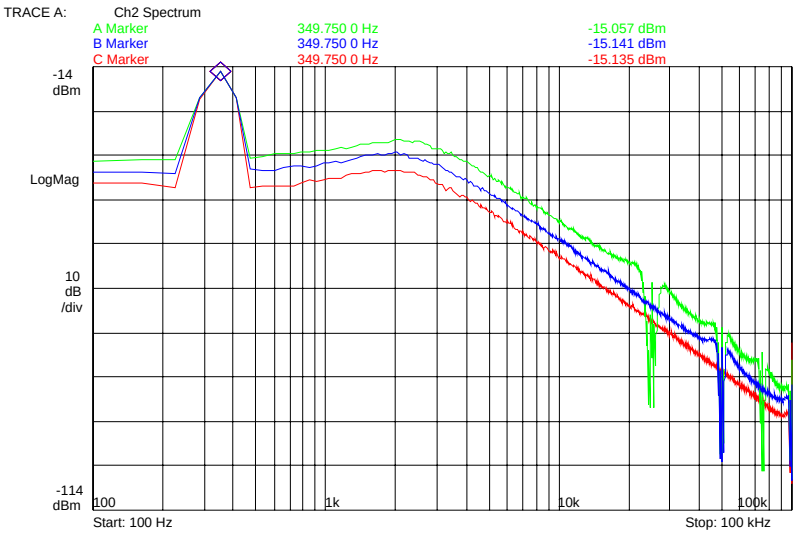


It can be seen that the sampled model has a wider bandwidth and as a result the noise due to the PLL will be higher than for the continuous time model outside the loop bandwidth except in the regions close to the sampling frequencies and its harmonics where the PLL noise is heavily suppressed.

6. Sampled signals and noise in the PLL emulator

If a small signal is introduced along with the noise the effect on the signal and noise can be observed with different sampling frequencies. The measurements (Figure 14) show that the signal level remains unchanged as the sampling frequency is changed but, as before, the noise level falls by ~3dB every time the frequency is doubled. As before there are aliases either side of the sampling frequency and its harmonics but they are lost in the nulls.

Figure 14



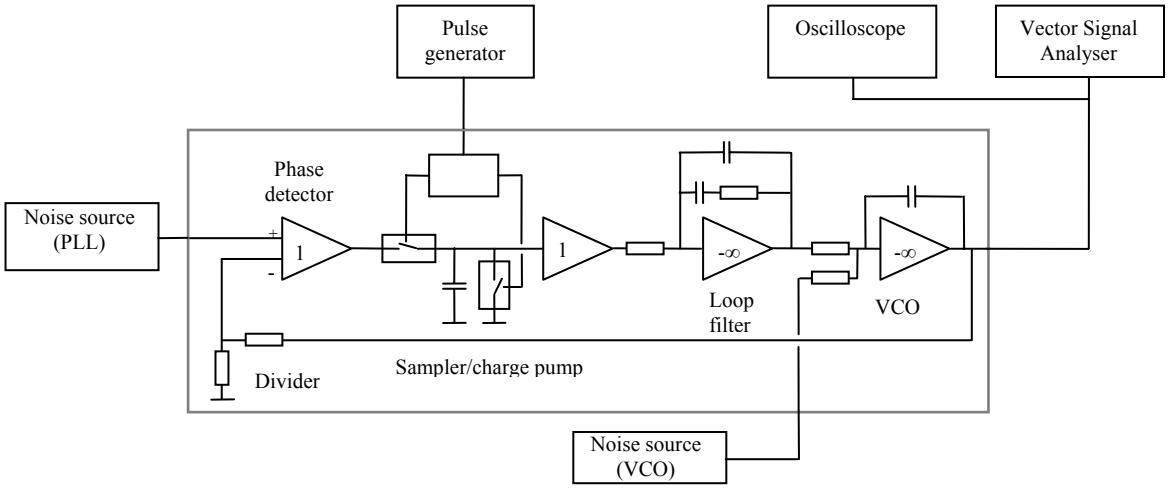
This result is as expected but is in contrast with our general experience of PLL ICs where the PLL noise increases by 3dB for every doubling of comparison frequency and this relationship usually holds true over many octaves. Some have tried to explain this by saying the charge pump is on twice as often so there is twice as much noise delivered to the loop filter [4,5]. However my belief is that the higher sampling rate is actually working in our favour. If we think about the case for the PLL and surmise that the PLL noise is due to timing error either at the divider input buffers or in the reference or feedback dividers, then if we double the frequency for the same timing error we would expect, from FM theory, the noise to be 6dB higher. But because of the phase detector's sampling action we get an improvement of 3dB. The net result is a 3dB increase in noise for each doubling of the comparison frequency.

7. Investigating noise sources in the PLL

One of the main sources of noise in a PLL is the in-band noise due to the dividers or phase detector. These can be difficult to separate in many PLLs though some manufacturers provide test modes that allow signals from the dividers to be routed to an output pin where they can be measured. In-band noise can easily be emulated in the base-band circuit by applying broadband white noise to the input and observing the output signal. If 1/f noise is an issue this can also be simulated by applying noise with a 1/f profile to the input. The other major source of noise is the VCO noise. This tends to have a flat profile at large offsets from the carrier. At intermediate offsets the noise has an f^{-2} profile and then at some lower frequency this rises to an f^{-3} profile. Oscillator noise with the f^{-2} profile can easily be added by summing white noise into the loop at the input to the integrator that emulates the VCO. This noise appears at

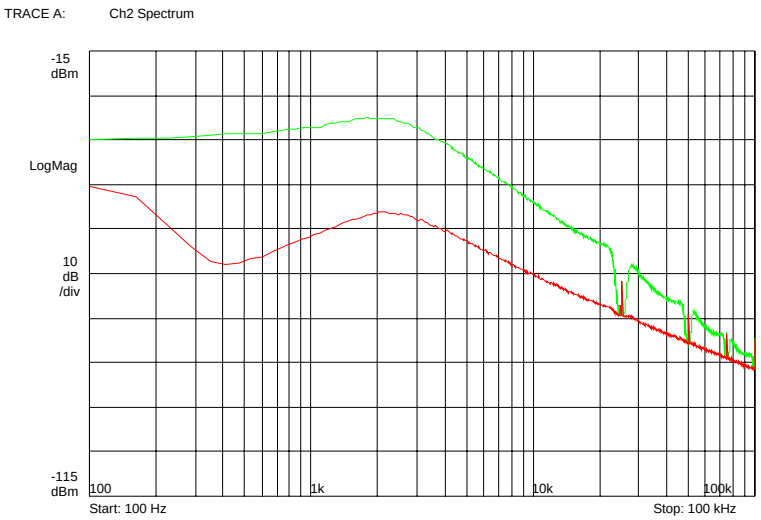
the output of the integrator with an f^{-2} profile. An oscillator with an f^{-3} region can be simulated by applying a shaped noise profile by summing noise with an f^{-1} profile to the white noise at the input. This noise can either be generated by analogue shaping or generating it digitally. The effect of each type of noise is easily demonstrated by applying a noise signal at the appropriate point.

Block diagram of set-up for demonstrating PLL noise sources



In Figure 15 the upper trace (green) shows the result when the in-band noise is significantly higher than the VCO noise at the loop bandwidth. The lower trace (red) shows the contribution due to the oscillator when the noise source is set to make the VCO noise low compared to the PLL noise as was the case in the test PLL. The general profile of these traces agrees well with those produced by calculation. The tendency for the VCO noise to rise close to DC is due to the sampling frequency feed-through aliasing to DC, and the limited resolution bandwidth of the measuring instrument.

Figure 15



In Figure 16 the noise due to the oscillator has been increased so that it becomes comparable with the PLL noise at ~50kHz. The nulls at the sampling frequency and its harmonics are still present but much less evident. The noise beyond 25kHz is being affected by the noise due to the VCO and by the time 100kHz offset is reached the noise is dominated by the VCO. The blue trace shows the response if there were no contribution from the oscillator.

Figure 16

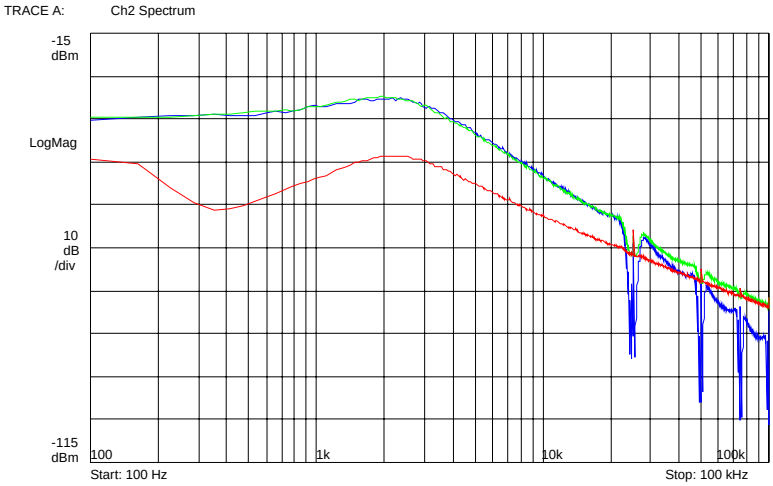
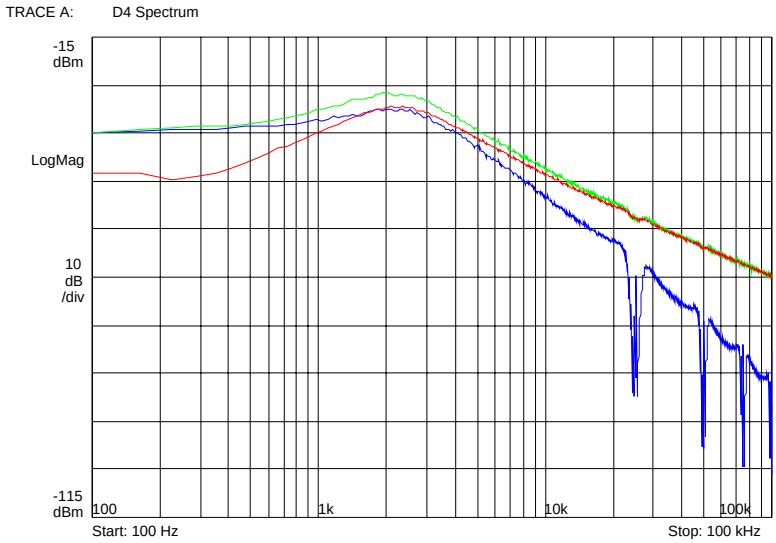


Figure 17 shows the case when the VCO noise is comparable to the PLL noise at the loop bandwidth. It can be seen that the peak at the loop bandwidth is higher due to the VCO noise and that there are still small disturbances to the noise at the sampling frequency and its harmonics even though the VCO noise is much greater than the PLL noise.

Figure 17



8. Phase response

The final aspect of the simulation to be verified with the base-band circuit is the phase response. Figure 18 shows the calculated response and Figure 19 shows the measured response. The two are very similar although in the measurement there is some disturbance to the phase at the sampling frequency. This is most likely due to the presence of sampling clock breakthrough which is much larger than the signal that is being measured in the nulls.

Figure 18

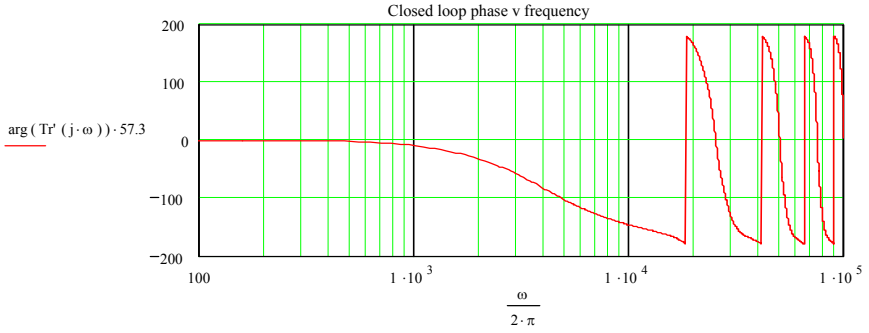
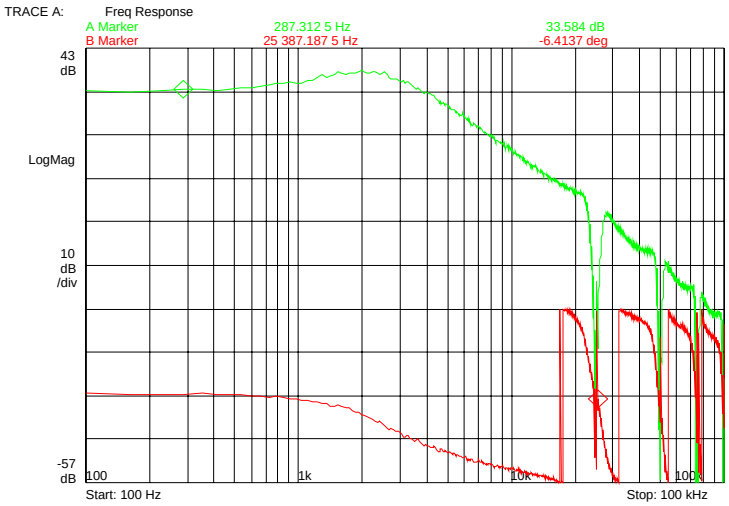


Figure 19



Conclusion

The construction of a base-band circuit that emulates the behaviour of a PLL has provided a reliable model for understanding some aspects of PLL performance. The measurements indicate that the mathematical equations developed in reference [3] are correct and can therefore be used to predict the phase noise performance of PLLs where the loop bandwidth is wide compared to the comparison frequency, typically where the comparison frequency is less than ten times the loop bandwidth. It also confirms that the simulation packages, provided by the PLL IC manufacturers, do not represent the true performance under these conditions. In the course of making the measurements some light has fallen on the effects of sampling and produced an explanation for the 10log f_c in-band noise characteristic of PLLs that fits neatly with sampling theory.

References

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