A 5 Gsps 8-10 bit ADC Platform Concept for RF and Instrumentation Applications

François BORE,
e2v, avenue de Rochepleine, BP123,
38521 Saint-Egrève Cedex, France
www.e2v.com

ABSTRACT

In this paper we will introduce a 5Gsps ADC platform for RF and Instrumentation based on programmable interleaving of four fast ADC cores on a single chip. Analogue digital converter is a known bottle-neck in the RF reception chain and is considered the keystone for accurate digital instrumentation.
In order to process ever increasing bandwidth signals, there is a pressing demand for faster Analogue to Digital Converters , one popular solution to deal with this demand is the use of time domain interleaving, yet time domain interleaving requires many precautions or implies tremendous digital post-processing overhead.
We will discuss the interest and limitations of time domain interleaving of ADCs to build a faster giga-sample ADC, we will also discuss the features needed on elementary ADCs to perform proper time domain interleaving: that is interleaving with yield results close enough to the one obtained from a non interleaved fast ADC so that no further digital post-processing is needed to make for imperfections of time domain interleaving.
Based on this discussion we will explain how we have oriented e2v's design to provide a 5 Gsps versatile ADC platform which will make things much more easy for system designers, thanks to build in features allowing readily interleaving without extra analogue devices, digitally controlled by a standard industry SPI (Serial Peripheral Interface) We will also explain our technological choices.
Finally we will illustrate our discussion with results obtained on e2v quad 8 bit ADC in production and on next generation 10 bit demonstrator.

Introduction

Over the last decade there has been an increasing demand of signal bandwidth for RF transmission due to the increase of payload request in both civilian application (e.g direct internet via satellite, high definition video…) and military application (electronic warfare, field communications…) leading to what is commonly called broadband communications.
Furthermore there is a constant demand to push digital world higher in the reception chain thus suppressing costly analogue stages (mixer and filter) and coding signal on ever higher intermediate frequencies.
All this is aimed to Software Define Radio which is the new Holly Grail of RF transmission, and should be to this century what super heterodyne demodulation was to last century. What is at stake is to get modulation schemes independent of hardware implantation of reception stages, and to be able to modify modulation scheme by a mere reprogramming of digital processor.
In the same way we observed a race to sampling rate in the instrumentation market (A.T.E, D.S.O etc..)
Such a target puts tremendous pressure on the joint between Analogue and Digital worlds, the Analogue to Digital Converters (ADC). On the same way considering the emission path, the logic consequence of software defined radio is the use of Digital to Analogue Converters based arbitrary waveform generator to drive the last mixer and power stage, therefore the same pressure is put on DAC designs, but this is not the object of this paper.

What is the consequence on this trends on ADC requirements?

The most straightforward consequence of these new demands , interpreted through Shannon-Hartley's theorem is the increase of accuracy (SNR) or the increase of sampling rate, or both. In this paper we will discuss the increase of sampling rate with minimal degradation of SNR.

There are two ways to increase sampling rate of ADCs: time interleaving of "reasonably fast" ADC or building a faster ADC on a faster process. Each solution have of course drawbacks and advantages, we have developed both solutions for different applications. In this paper we will focus on time interleaving of ADCs, and requirement at ADC level and/or at system level to perform proper time interleaving. We will also see why massive interleaving of "slow" ADC is not such a good idea.

Time interleaving of ADCs principle

Time interleaving of ADC is a very seductive concept yet its not so obvious to obtain acceptable results, we will see why. The principle is to used m ADC (for practicable reason m is generally a power of 2) to convert the same signal at the same sampling rate f_s but with sampling instant shifted of p/m (where p is individual sampling period, that is $p=1/f_s$), in order to get an equivalent ADC sampling at $f_{seq} = m \, . \, f_s$.

In a perfect world this would work very well, but unfortunately we are in a real world with many nasty effects such as component matching, noise, phase uncertainty, and even some times different thermal drift. To achieve a correct time interleaved ADC (or TIADC, result of the time interleaving of m ADCs) all these issues must be addressed.

First of all we must agree on what is a correct TIADC . A correct TIADC should give result compliant with the system requirement, as would yield a simple fast ADC, if performances are degraded by interleaving they should be recoverable through moderate digital processing overhead (that is no useful information should be lost).

What are the requirement for interleaving ? At first order interleaving requires gain matching, offset matching and phase alignment of the interleaved channel. This requirements must be fulfilled over the full frequency range which means that bandwidths of the different channel should also be matched , or that input must be kept well below bandwidth, so that gain are actually matched over the input frequency range.
For clarity we will illustrate the cases of 4 interleaved ADCs with a pure sine as input, with ideal response, raw converted signals (1024 point per ADC, and zoom on one input signal period), and reconstructed signals (1 full period, and zoom on critical points). Then we will se impact on these plots and investigate consequences imperfections in the interleaving in each case. Figures hereafter are given with an 8 bit ADC, and an individual over sampling ration close to 2.

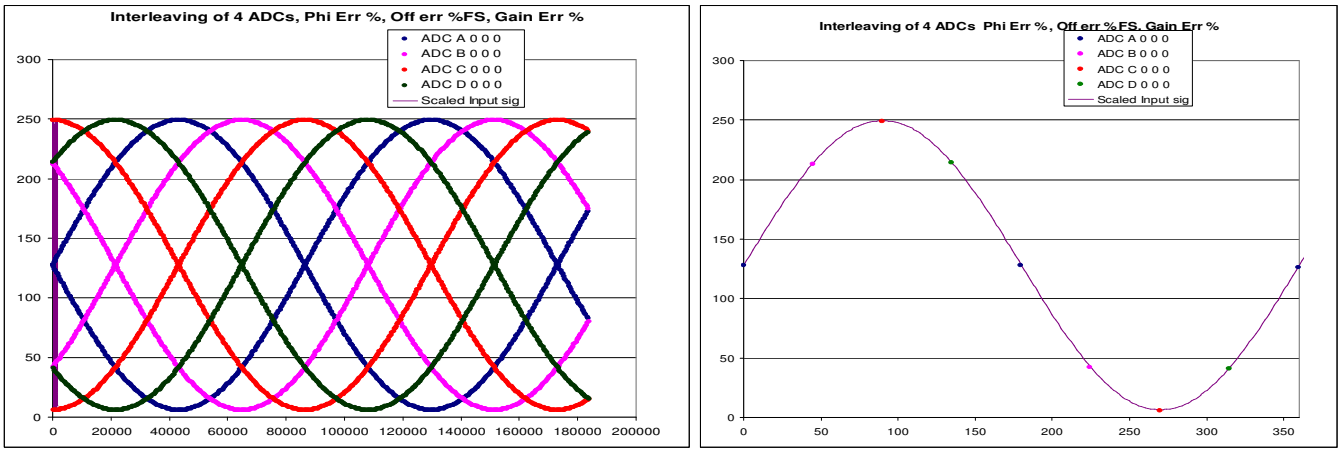

Fig 1: raw ideal 8 bit converted signal (1024 point per ADC, and zoom on 1st input period).

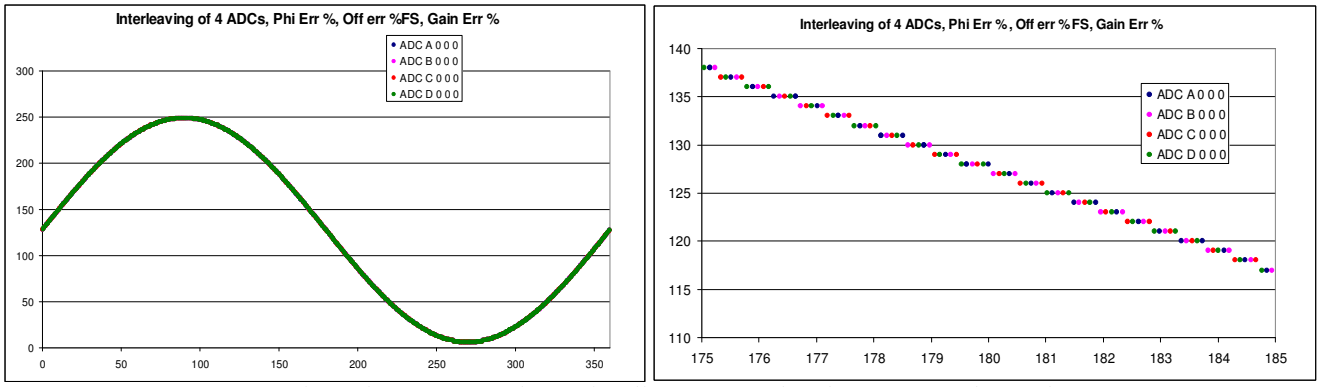

Fig 2: Interleaved reconstructed signal (full input period and zoom around 180 degrees).

Source of degradations and proposed solutions:

There are two kinds of sources of degradation :

1. deterministic degradation which are easy to compensate in analogue world or to process in digital world , for instance offset, gain, INL or sampling instant misalignment.
2. statistical random degradations: for instance thermal noise in the different signal paths or uncorrelated phase noise for the different sampler.

We will first address the deterministic degradation and then we will see how to minimize effect of statistical degradations.

Deterministic degradations

Offset mismatch errors

The first possible imperfection is offset mismatch of the 4 channels, this can be compensated in analogue world thanks to the (digitally controlled) offset tuning of the ADCs or in the digital world in the DSP (which implies slight overhead: adders), to avoid digital overhead it is always preferable to perform this correction in analogue world.

If interleaving is done amongst different chips, differences in thermal management of the different chips may requires offset recalibration when system temperature changes. In the case of a 2 or 4 channels interleaving using EV08AQ160, this is not needed thanks to the perfect temperature tracking of the four ADCs on the same chip, and thanks to the flat response over temperature of offset tuning.

The effect of offset mismatch errors is independent of the over sampling ratio (OSR), it is the same on any point of the curve. Offset mismatch errors don't scale with input amplitude.

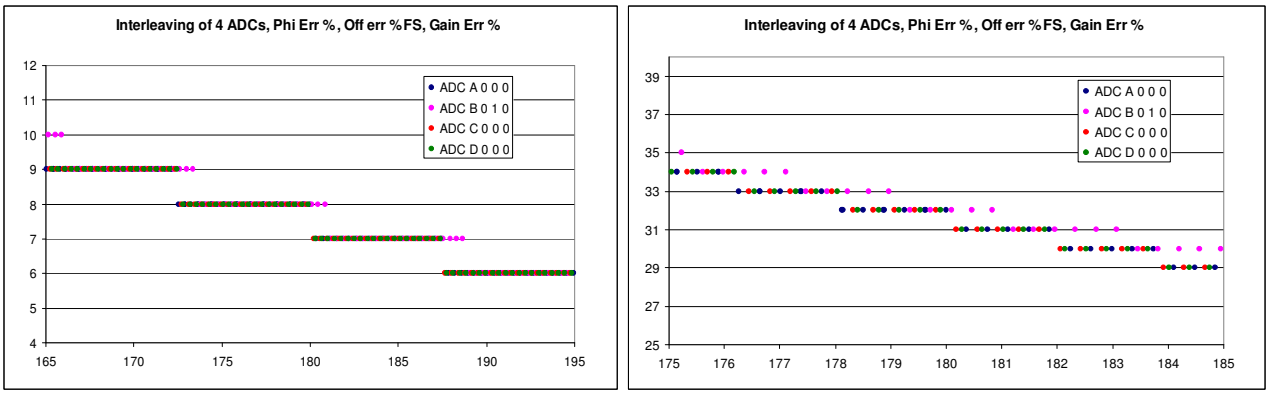

Fig 3 : Effect on reconstructed signal of a 1% Full Scale Offset error on B channel for 4bit and 6bit resolutions.

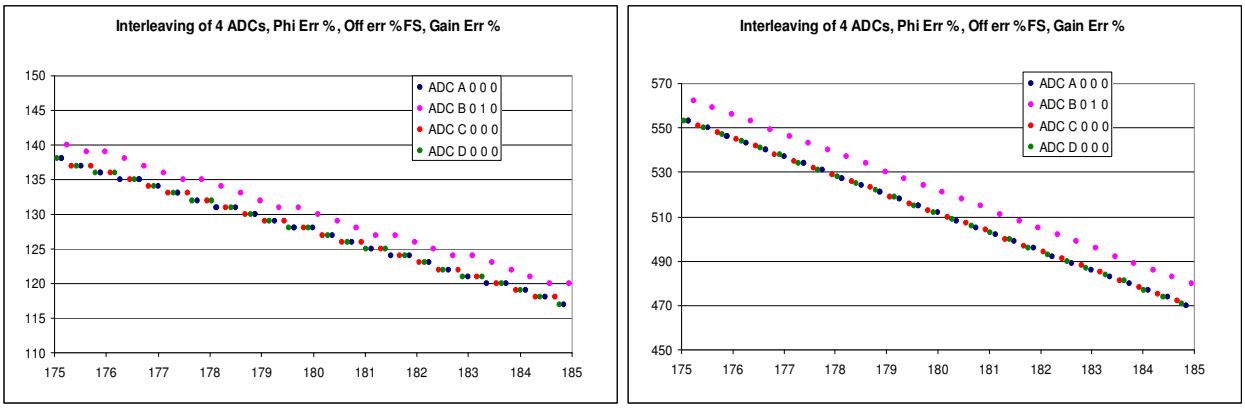

Fig 4 : Effect on reconstructed signal of a 1% Full Scale Offset error on B channel for 8bit and 10bit resolutions.

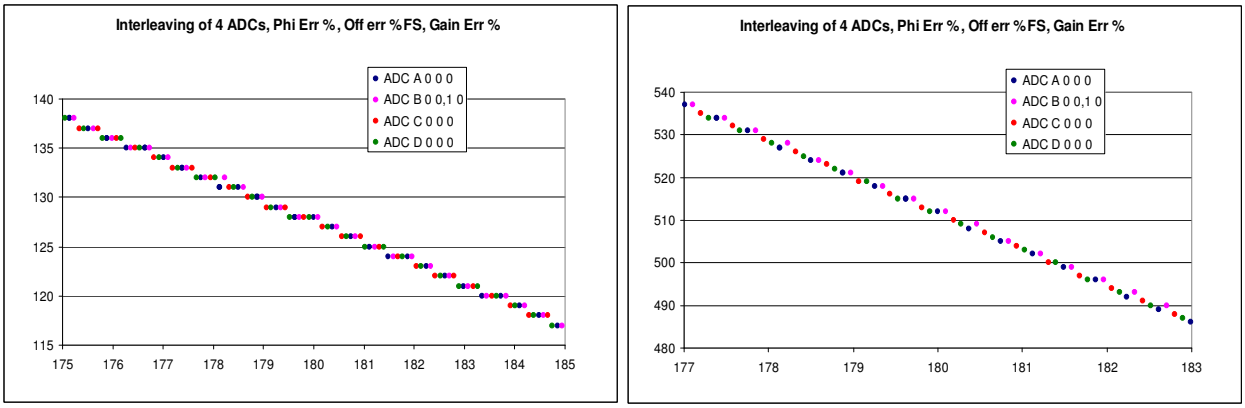

Fig 5 : Effect of a 0.1% Full Scale Offset error on B channel for 8bit and 10bit.

If offset matching errors are close to or larger than one LSB, they are clearly visible on reconstructed signal, otherwise they might be wrongly interpreted as quantization errors. If they are of same order or larger than thermal noise, the SNR of interleaved system will be degraded regarding the SNR of a single core system. Even smaller errors have clear effect on signal spectrum, since they are deterministic and their energy is concentrated in the same frequency slot (clock related spurs at f_s or $n.f_s$ depending of the error pattern, but independent of input signal amplitude), thus having an impact on SFDR.

We can see clearly that offset matching requirement depends on ADC resolution.

E2V's EV08AQ160 includes digitally controlled (through SPI) offset tuning fine enough (that is with of a resolution between one fifth and one tenth of a LSB) so that no further digital processing is needed for offset cancellation. Further more with the EV08AQ160 only one input is used for interleaving of the 4 cores, that is absolute offset error of the external preamplifier or front-end will not have any effect on interleaving process since the same error will be seen by the four ADC cores.

Gain mismatch errors

The second possible imperfection is gain error mismatch between the different interleaved channels. Once again this can be compensated in the analogue world thanks to the (digitally controlled) gain tuning of the ADCs or in the digital world in the DSP (which implies larger overhead than for offset error cancellation: multipliers), to avoid digital overhead it is always possible to perform this correction in analogue world.

If interleaving is done amongst different chips, differences in thermal management of the different chips may requires offset recalibration when system temperature changes. In the case of a 2 or 4 channels interleaving using EV08AQ160, this is not needed thanks to the perfect temperature tracking of the four ADCs on the same chip, and thanks to the flat response over temperature of gain tuning.

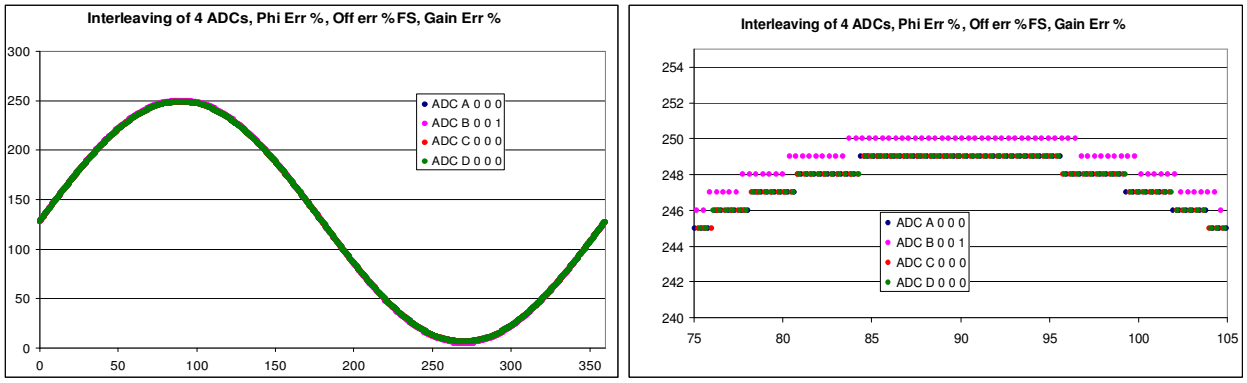

Fig 6: effect of a 1% Gain error for Channel B on interleaved reconstructed signal 8bit resolution.

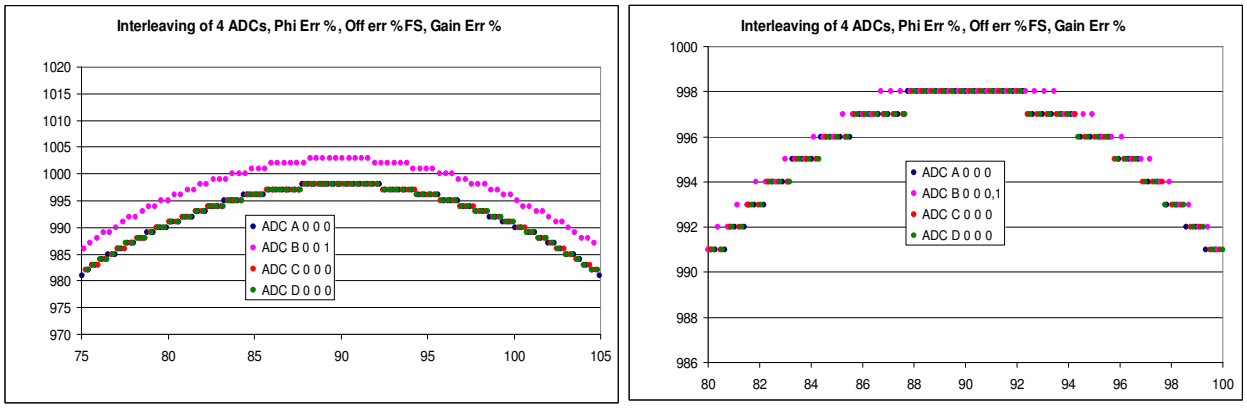

Fig7: effect of a 1% and 0.1% Gain error of channel B, on a 10 bit interleaved ADC.

The effect of gain mismatch errors is independent of over sampling ration (OSR), gain error scales with signal amplitude, this is why gain errors are more visible when input is closer to full scale. Gain mismatch errors are visible on reconstructed signal when resulting full scale relative errors are close to or larger than one LSB, smaller errors might be erroneously interpreted as quantization errors. Anyway even smaller errors have a clear spectral signature since they are deterministic and their energy is therefore concentrated in a few frequency slots. (expliquer les spurs du spectre).

E2V's EV08AQ160 includes SPI digitally controlled gain tuning of each channel fine enough (that is full scale adjustable with a precision of one fifth of a LSB) so that no further digital processing is needed for relative gain error cancellation. Further more with the EV08AQ160 only one input is used for interleaving of the 4 cores, that is absolute gain error of the external preamplifier or front-end will not have any effect on interleaving process, since the same error will be seen by the four ADC cores.

Phase alignment errors

The third possible systematic error in interleaving is what we will call phase alignment errors (that is deviation from ideal phase of the clocks of individual interleaved ADCs). In theory sampling instants are evenly spaced on the phase circle, but due to physical limitation this is of course not entirely true. The clock phase error of individual interleaved ADC have of course impact on overall conversion.

The clock phase error impact is divided by the OSR of individual ADCs, this is why interleaving of many "slow" ADCs implies strong constraints on phase calibration, and it often more efficient to interleave a small number of reasonably fast ADCs.

Phase alignment can be performed at system level in analogue world (and can be very painful is special features have not been embedded in ADCs to make things easier), or in digital world in the DSP (interpolation between points to compute data points at ideal instant, and processing of the said data points) which would imply a huge digital overhead, with a training phase on a probe signal.

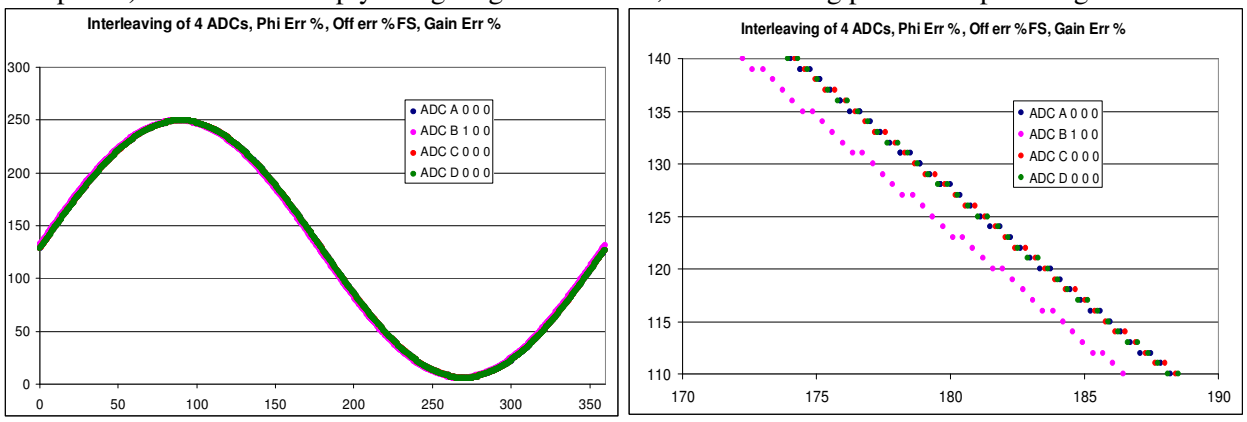

Fig 8: effect of 1% phase error in B channel clock, on a 8bit Interleaved ADC with individual OSR close to 2.

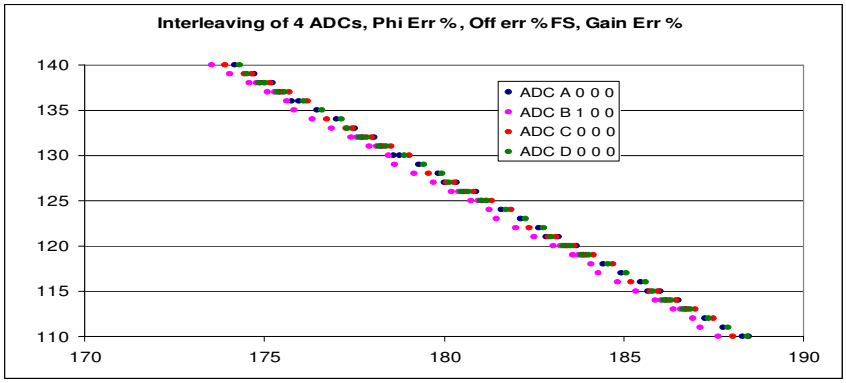

Fig 9: effect of 1% phase error in B channel clock, on a 8bit Interleaved ADC with individual OSR close to 8.

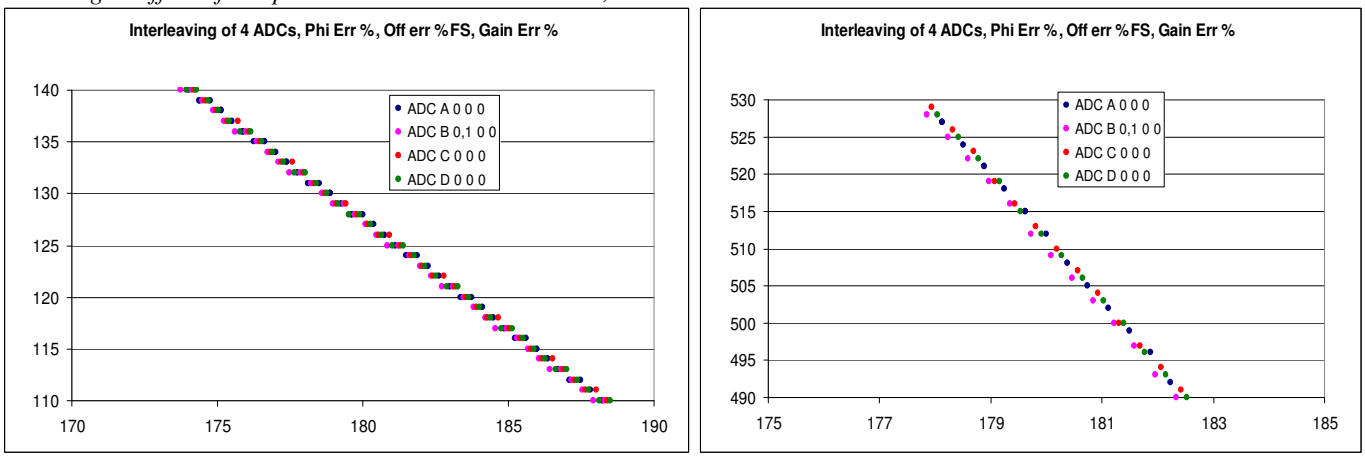

Fig 10 effect of 0.1% phase error in B channel clock, on 8 bit and 10 bit Interleaved ADCs with individual OSR close to 2.

In order to avoid digital overhead phase must be adjusted very accurately in the analogue world : the phase errors divided by the OSR regarding the fastest signal to convert, multiplied by the number of quantified level must much smaller than one, otherwise the effect would be clearly visible on reconstructed waveform.

That means that for a eight bit with an individual OSR of 2 (that is each ADC operating in first Nyquist zone) the individual phase errors must be much smaller than 1/(2pi*256/2) cycle, or 0,45

degree. Considering a 1 GHz clock and a 500MHz input, the sampling instant error should be smaller than 1.24ps.
Once again spectral signature is visible even for small phase shift since it's a deterministic phenomenon with energy concentrated in the same frequency slot.

Phase adjustment and clock distribution is always something very tricky at system level this is why we have chosen a robust solution in EV08AQ160 for interleaving the 4 ADC cores from a single double speed external clock. Each internal clock is adjustable by steps of about 120fs, digitally controlled through the SPI.
Further more the use of a double speed external clock reduce the added jitter added by the ADC thanks to steeper edges seen by clock input buffer.

If interleaving is done amongst different chips, differences in thermal management of the different chips may requires offset recalibration when system temperature changes. In the case of a 2 or 4 channels interleaving using EV08AQ160, this is not needed thanks to the perfect temperature tracking of the four ADCs on the same chip.

Here after are examples of phase misalignment effect on reconstructed signal at various individual OSR, and with different ADC resolution. We can see clearly that the susceptibility to clock phase misalignment increases when OSR decreases.
(insérer ici les courbes avec phase mismatch)

INL mismatch errors

The last possible deterministic interleaving imperfection is INL mismatch between the different channels. Of course the constraints on individual ADC's INL are the same as it would be on a single fast ADC. In fact the interleaving of m ADCs is a rather good thing considering global INL since each ADC contributed for one m^{th}, we have an averaging of INL. As a consequence, SFDR produced by m interleaved ADCs can be better than SFDR resulting from an elementary ADC, since each ADC contributes for one m^{th} of the energy, and it is likely that spectral spurs related to the individual INL profiles will not be coincident. Unfortunately things are not so good regarding reconstructed signal and noise floor.

A good interpretation is the following: INL can be considered as code dependant offset, therefore individual INL mismatch between interleaved ADCs exceeding thermal noise level will have direct visual effect on reconstructed signal.

INL is mainly a statistical issue due to component matching in the first stage(s) of the quantifier. The INL amplitude can be predicted before fabrication knowing matching constants of the devices used, but its actual profile for the random part of course can't be predicted before fabrication.

If the signal have time enough to settle through the quantifier (quasi static behaviour assumption, which is verified thanks to the use of a front end T/H before each quantifier) then the INL profile of a quantifier is fairly stable against clock frequency and input frequency. This is why we put the INL issue in the category of deterministic phenomenon, indeed from an application point of view its impact is deterministic.

This is a very good piece of news because it makes possible, for demanding applications, INL improvement either in analogue world (INL calibration, introducing digitally controlled offset at critical points of the quantifier first stage(s) to compensate natural offset due to component matching), our in digital world with a Look Up Table in the DSP (in the case of interleaving, each individual ADC should have its own look up table, this is manageable for moderate interleaving, and becomes a nightmare for massive interleaving, especially for real time applications).

E2V's quad 8 bit ADC EV08AQ160 includes SPI digitally controlled INL tuning functions allowing to reduced the INL of each individual ADC INL down to +/- 0.3LSB, which is below thermal noise level. As a consequence for demanding applications Look Up Table for INL improvement are not needed in the DSP thus simplifying design.

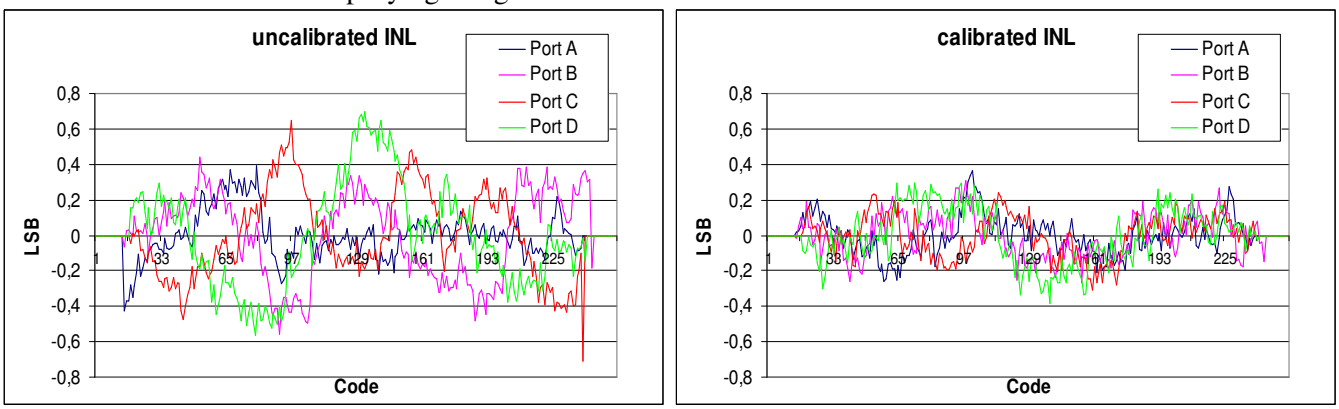

Fig. 11: Individual INL of the 4 channels of EV08AQ160 before and after calibration.

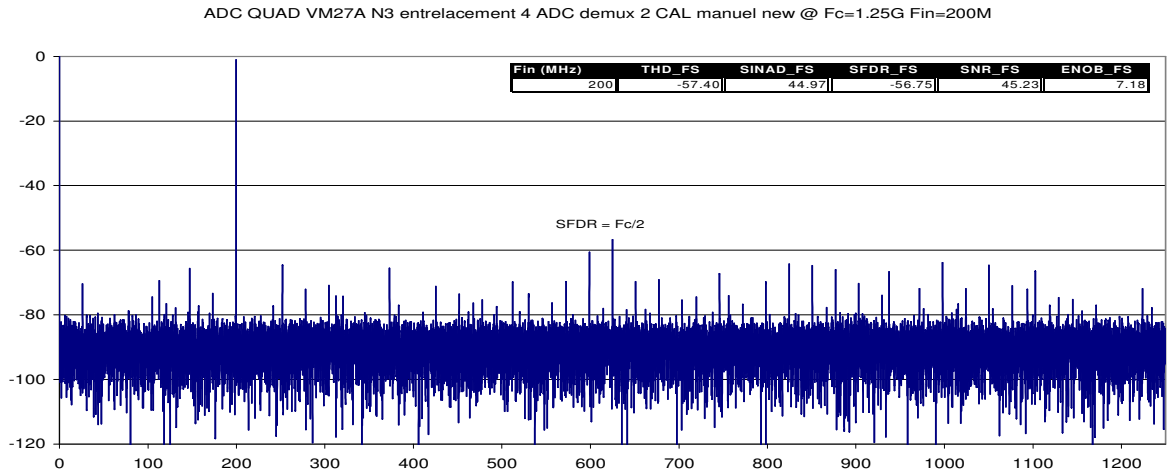

Fig 12: spectrum after interleaving of 4 channels of EV08AQ160 for 200MHz input

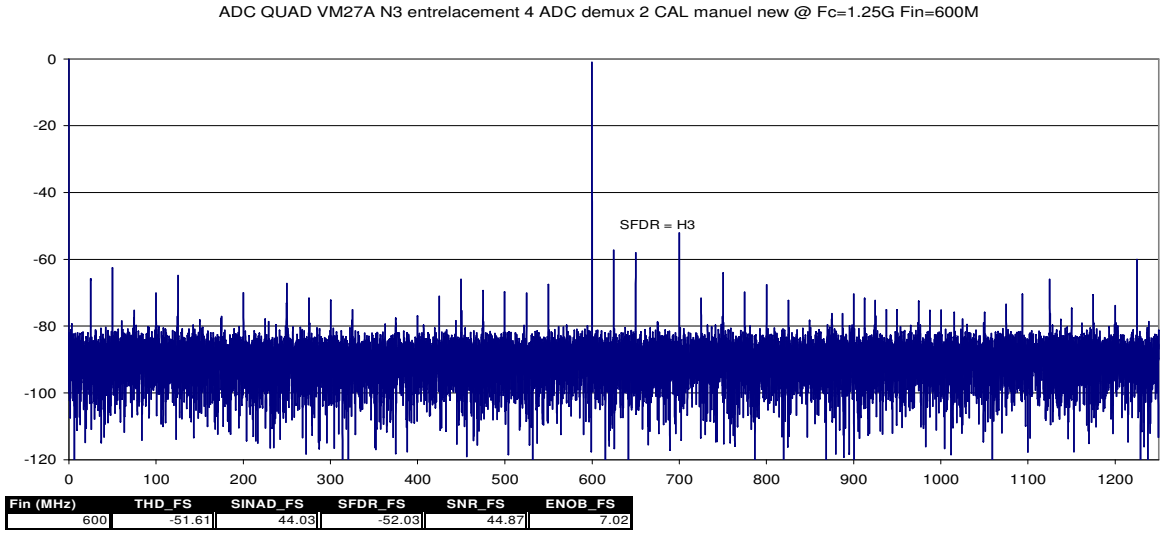

Fig 13: spectrum after interleaving of 4 channels of EV08AQ160 for 200MHz input

Statistical random degradations

Some imperfections are not deterministic and can not be fixed by deterministic solution, they are link to thermal noise or jitter phenomenon, nevertheless some precautions at ADC design level or at system design level can be taken to reduce their effects.

For each ADCs noise can be considered as randomly added offset error at each sample.

For each ADCs time Jitter can be considered as randomly added phase error at each sample.

The noise collected by each individual ADC will contribute to the overall noise of the interleaved ADC, and in the same way the clock jitter of each individual ADC will contribute to the global jitter of the interleaved ADC.
As a consequence jitter constraints for the clocks of interleaved ADC are as stringent as jitter constraint of the clock of a full speed ADC, which means that power used for clock drivers in an interleaved ADC system increase linearly with the number of ADCs yet each individual ADC operates with slower clock(see jitter added in a buffer depends on input referred noise divided by input edge steepness, as a consequence edge of slow clocks must be kept as sharp as edges of a single full speed clock). This is why massive interleaving is not a good solution when targeting a good resolution.

One solution to deal with jitter and clock precision in an interleaved system is to use an external front end T/H at full sampling rate of the system and let each individual ADC resample the output of this T/H. This is often not a practical solution for the following reasons:

- Availability of such a device.
- Thermal noise added by such a device if available.
- Difficulty to distribute properly the output of the T/H to all the ADCs.
- Power budget of such a solution.

The other solution is to interleaved a small number a reasonably fast ADCs with front ends good enough so that external T/H is not needed.
The first idea, when you want an interleaved ADC system to behave as close a possible as a true equivalent high speed ADC is to chase uncorrelated sources of noise and jitter between the different ADCs. That is to keep the clock path and analogue input path common to all the ADC as long as possible. When interleaving is done at chip level this is of course much easier than when interleaving is done at system level.

Another good idea is to keep the thermal tracking of the different ADCs as tight as possible, see otherwise the system would have to undergo calibration more often than wish able. When interleaving is done at chip level this is of course much easier than when interleaving is done at system level.

Keeping all this in mind in mind we have developed our quad ADC platform, taking car of all the interleaving overhead on chip so that the system designer don't have to burden with all that stuff.

A build in cross point switch allows to drive the 4 ADC cores from a single analogue differential input, it is controlled through the SPI.

Clock distribution for interleaving by 2 our by 4 is managed at chip level from a single external clock operating at double individual sampling frequency, and is controlled through the SPI. The use of an external clock operating at double sampling rate allows for a better internal jitter management and for internal clock tree simplification in the three possible configurations (no interleaving, two folds interleaving our four folds interleaving) which results in optimized jitter and power dissipation.

Gain, offset and phase of each individual ADC of EV08AQ160 are digitally adjustable thanks to 8 bit DACs controlled by the SPI. In each case the step of adjustment is fine enough to allow for results in interleaved modes close to results in non interleaved mode.

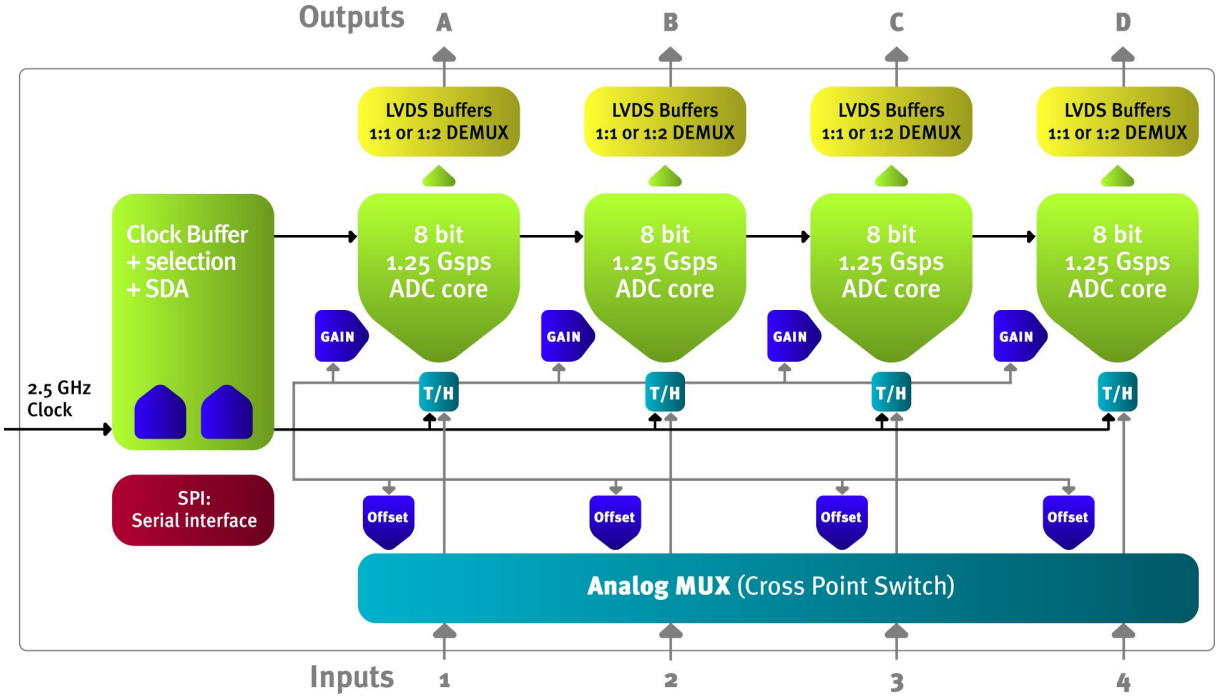

Fig14: Block diagram of EV08AQ160

For the 10 bit demonstrator EV10AQ190, gain offset and phase of each individual ADC are adjustable with 10 bit DACs controlled by the SPI, with finer step of adjustment to take in account the higher resolution targeted.