A review of amplifier stability analysis using modern EDA tools

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Abstract

Modern design tools possess many utilities that can be employed to explore the stability behaviour of circuits. These range from invasive techniques such as probes and N port elements which are inserted into the circuit schematic, to non-invasive methods which involve calculation of the circuit matrices … for example K factor calculations and NDF techniques. This paper discusses these methods and will attempt to put the various techniques into perspective so that designers are able to select the most appropriate tool for their investigations.

Introduction

Stability analysis techniques need to be applied to a large class of circuit topologies. These range from single device gain stages with active bias, self-biased devices to multiple device amplifiers using complex cascade and or parallel amplifier arrangements. Techniques are needed for stability analysis of these amplifiers for DC operating point analysis, commonly called local stability analysis. If the amplifiers are driven close to or into compression then nonlinear stability analysis techniques are also needed to complement the DC stability checks.

The application of the linear stability analysis techniques provide the designer with insights into potential source or load terminations or feedback margins that may indicate potential instability leading to some form of oscillation. Whilst these techniques provide some awareness into the potential startup of the oscillation, nonlinear time domain techniques are needed to establish whether a sine wave, square, triangular wave shape is the stable oscillation mode, if such a stable condition is indeed possible. The amplifier designer of course is not interested in the wave shape of the potential oscillation; his concerns are not abstract, rather they focus on providing a system block that delivers the required stable gain without the active devices destroying themselves!

1. Linear Stability Analysis

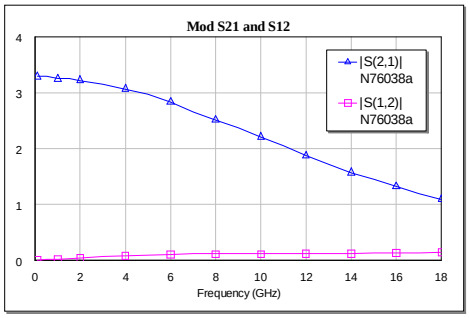
It is generally understood that stability analysis using stability circles or K factors is incomplete. These well-established techniques tell the designer whether the application of a specific combination of source and load termination will or will not create a right-hand-plane (RHP) pole. Another way to express this is … An unloaded Two-port which has no intrinsic poles in the RHP will remain stable when terminated if and only if K>1 and B1 >0. The role of K is limited to the investigation of I/O terminations that do not give rise to instability. The stability of the un-terminated system needs to be investigated by employing other techniques.

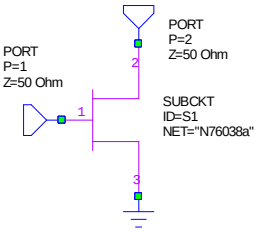
Of course, for oscillator design, the behavior of the poles; that is their initial locations and their power sensitive migration or evolution is critical, and is the essence of robust oscillator design. The amplifier designer just needs to know RHP poles exist and what circuit topology and or component parameter changes are needed for their removal.

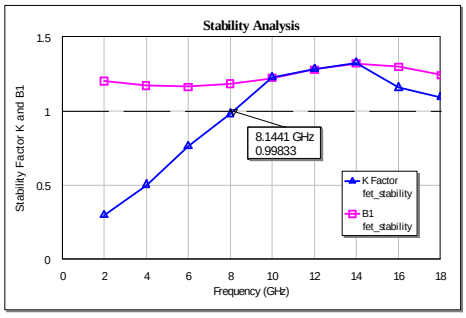
The paper by Platzker et al [1] makes an interesting observation that the design problems that make use of K and B1 factors is similar to the classical control problem addressed by Nyquist, in that both techniques focus on connecting inherently stable building blocks to construct more complex systems. In the case of cascading two ports one examines the termination

behavior and in the case of the feedback system one closes the loop. As mentioned before, in both situations the internal stability of the building blocks are to be established by alternative methods.

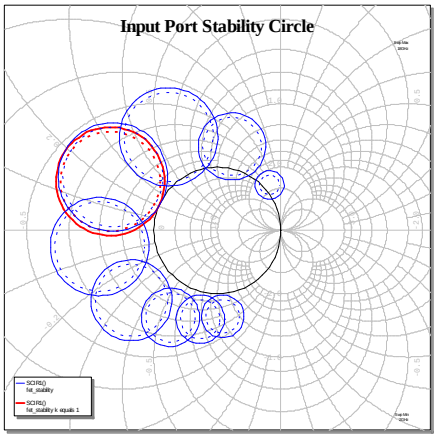
Before moving on to discuss the internal stability of amplifiers it is useful to quickly review the use of the K factor and stability circles. A simple observation can be made, a device that exhibits internal feedback maybe potentially unstable. Below we have plots of Mod(S21(f)) and Mod(S12(f)) for an NEC FET.

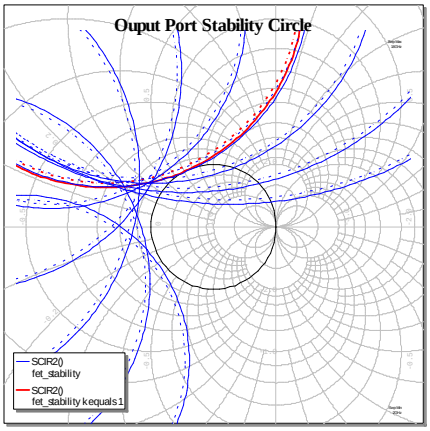




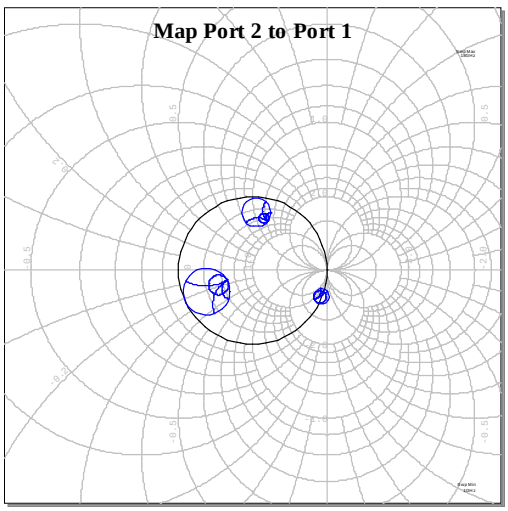


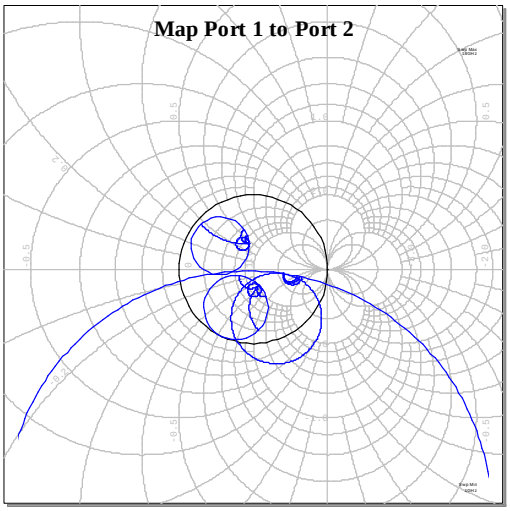
The plots of K and B1 illustrate that this device is potentially unstable below 8.1 GHz. This observation will be made with all transistors of this class irrespective of manufacture! The internal feedback is the result of collector(drain)-base(gate) capacitance or series parasitics between the common electrode emitter (source) and the ground node. Below we see the Input Port and Output Port stability circles. The circles that overlap the gamma = 1 boundary of the Smith Chart that are below the critical frequency (the Stability Circle at the critical frequency is coloured red) imply potential instability. Above the critical frequency the stability circles are found outside the gamma = 1 boundary of the Smith Chart.





The alternative to the Stability circle is the mapping circle … below we have three mapping circles on each I/O map, one below the critical frequency, one at the critical frequency and one above the critical frequency.





With the LHS graph above Γ_L is mapped to Γ_{in} using the following expression …

$$\Gamma_{in} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \quad \text{… (1)}$$

Here the entire load gamma constrained to the $|\Gamma_L| <= 1$ circle represented by a Smith Chart is mapped to the input gamma along tragetories that follow the constant resistance and reactance circles etc. The Γ_{in} appears as a distorted Smith Chart. Above the critcal frequency it can be seen that any impedance with a non-negative real part can be applied to one terminal and the other terminal will present an impedance that has a non-negative real part. Below the critical frequency it is observed that even connecting an impedance with a positive real part can cause the opposite port to exhibit negative resistance. This negative resistance if not supressed locally by a greater positive resistance could give rise to instability. The type of instability is controlled by the relationship between the resistive part (in this case negative) and the accompanying reactive environment.

3. Pole Zero analysis

The requirement that any of the system functions Z(s), Y(s), Vgain(s) etc. should not possess any poles in the RHS complex S plane originates from the time domain behaviour of systems defined by such poles. Poles and zeros are the special names we give to the roots of the system or network equations.

Linear time invariant (LTI) systems yield system functions that are collectively known as rational functions. That is

$$F(s) = \frac{N(s)}{D(s)} \quad \text{… (2)}$$

with the numerator N(s) and demoninator D(s) polynomials adhering to a set of rules governing rational functions [2].

The roots of D(s) defines system poles and the roots of N(s) define the system zeros. To establish the transient behaviour of a system the inverse Laplace transform of the system function needs to be calculated. The inverse Laplace transform can be either calculated using contour integration or by partial fraction expansion. The process of partial fraction expansion into known forms or more simple functions permits the inverse Laplace transform to be obtained by inspection from pre-built tables. In the example being considered F(s) can represent any of the system functions outlined above.

Let us consider a system or network with only first order poles, which we obtain from a partial-fratcion expansion of (2).

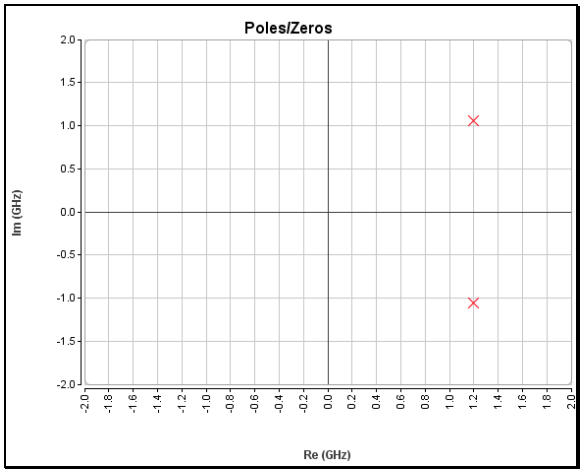
$$F(s) = \frac{K_0}{s-p_0} + \frac{K_1}{s-p_1} + \ldots + \frac{K_n}{s-p_n} \quad \ldots (3)$$

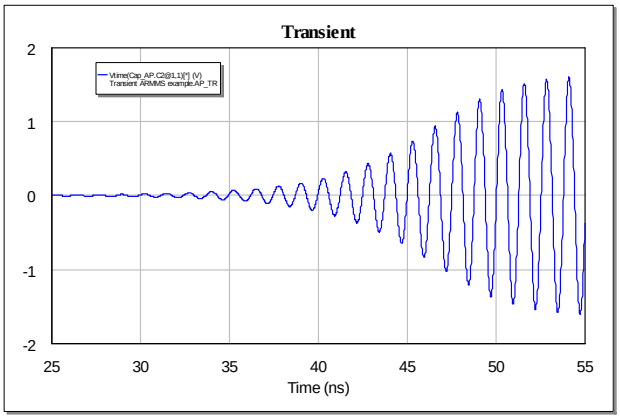
The inverse transform of F(s) is

$$f(t) = K_0 e^{p_0 t} + K_1 e^{p_1 t} + \ldots + K_n e^{p_n t} \quad \ldots (4)$$

$$= K_0 e^{\sigma_0 t} e^{j\omega_0 t} + K_1 e^{\sigma_1 t} e^{j\omega_1 t} + \ldots + K_n e^{\sigma_n t} e^{j\omega_n t} \quad \ldots (5)$$

With f(t), we observe that if the real part of a pole is positive, that is $\sigma_i > 0$, then the pole is found on the RHS of the complex s-plane. The corresponding term in the partial-fraction expansion $K_i e^{\sigma_i t} e^{j\omega_i t}$ is an exponentially growing sinusoid. In this example $\sigma_i = 1.2$ and the poles (complex conjugate pair) have been plotted below. The transient solution associated with this pole pair is also shown.





A detailed analysis of the pole zero description of the system provides the designer with insight into potential instabilites and the manner in which a system responds to impulses and step changes. These techniques are more commonly found in the design of control loops used in complex systems, but nevertheless provide a ready made and useful tool kit for RF and Microwave circuit designers as their designs become more sophisticated.

4. NDF and RR_T

With both the K factor analysis or the application of the inverse Laplace transform to examine potential instability, the characteristics of the network have been explored at selected terminals, both external and internal. The limitations of the K factor methodology have already been stated. The testing of a selection of user specified nodes for negative resistance is a valid approach and makes use of the fact that the denominators of the system functions regardless of which ever node is being tested share the same roots. But therein lays a problem. The poor selection of a test node may suffer from a de-sensitization. Large circuits possess complex patterns of poles and zeros making it important that the correct nodes are selected for testing to avoid numerical errors. An alternative approach is to examine the properties of the entire circuit matrix rather than the properties of specific nodes, in other words adopt a topologically global approach.

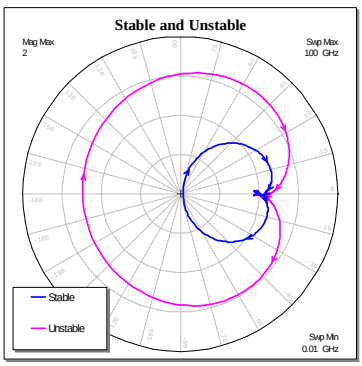
The system determinant describes fully the characteristics of the circuit. If there are odd-mode oscillations, there must be zeroes in the right half-plane (RHP). These can be found by solving the matrix equations. This method is not very efficient as the matrix can be very large. Another way to find the stability characteristics of the circuit is by investigating a function that is closely related to the circuit determinant. One such analysis is the normalized determinant function for a circuit NDF [1] which is defined below

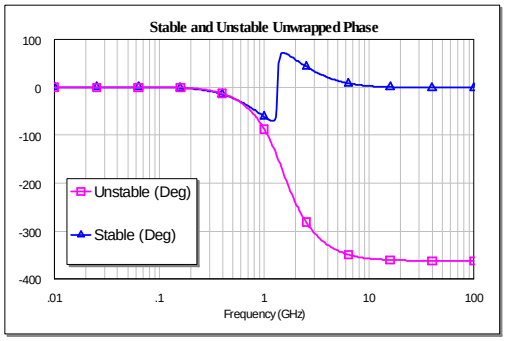
$$NDF = \frac{\Delta(s)}{\Delta_0(s)} \qquad \ldots (6)$$

where $\Delta(s)$ is the determinant of the network under investigation and $\Delta_0(s)$ is the determinant of a companion network which is identical to the network of interest except that all dependent active generators have been set to zero. The NDF approaches constant real values as frequency approaches zero or infinity. The circuit is stable if, on a polar plot, the NDF encircles the origin more times clockwise than counter-clockwise; (for example, if the unwrapped angle of NDF at the highest frequency is more than 360-degrees lower than the angle at the lowest frequency).

Unlike node and port-based linear measurements, the NDF computation requires access to active controlled sources (within elements) in the circuit. Active S-parameter data sets, or compiled linear models with controlled sources inside them do not allow this and are therefore not included in the measurement calculation.

The Polar plot below illustrates both stable and unstable circuits. The unwrapped phase equivalents are also included. When the circuits become complex the unwrapped phase plot is easier to examine.





5. Nonlinear Stability Analysis

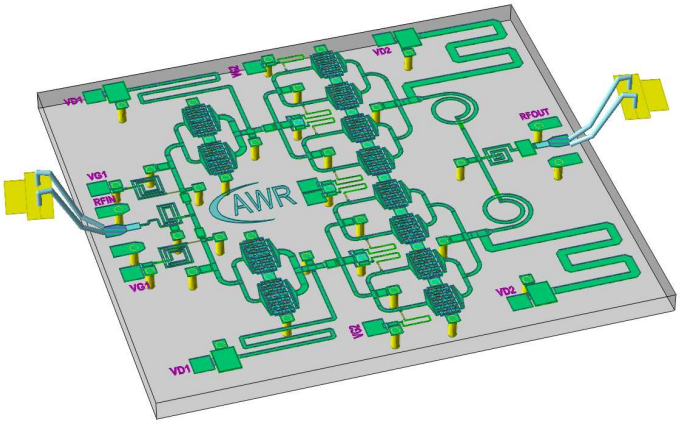
Having established that the amplifier is stable when the DC bias is applied the next task is to ensure that under all drive conditions the amplifier remains stable. As the magnitude of the input signal increases, the device nonlinearities start to be swept out and in affect certain regions of the active devices start to appear as parametric elements. The g_m of the transistor will vary with time and any of the junctions that exhibit voltage dependent capacitances will also vary with time. Some devices exhibit weak parametric affects … others are not so benign. In the context of low noise parametric amplifier applications, it is the time varying capacitance that provides the gain and it's C(t) characteristics is of course considered as vital. Whereas, for power amplifiers, such C(t) characteristics are seen not only as unwanted parasitics that limit bandwidth but as the primary element that gives rise to nonlinearity induced instability.

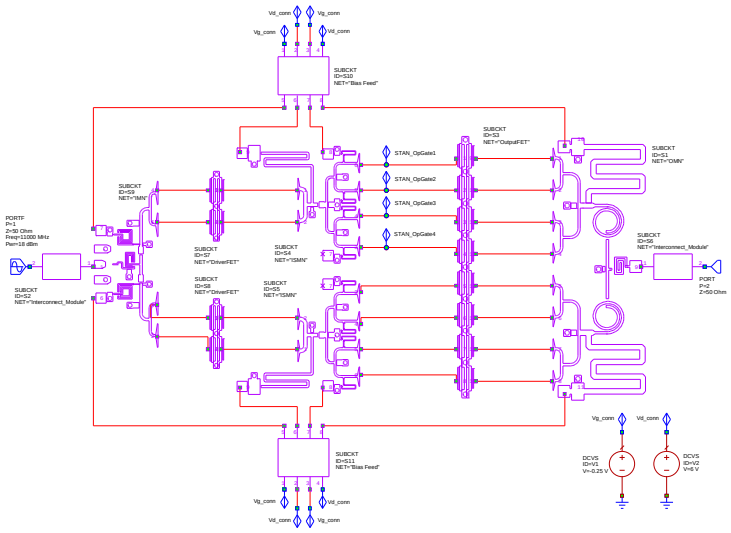
As explained in the previous sections, the Pole Zero analysis of a linear system gives insight into the transient behavior of the system during the linear phase of oscillation when RHP poles are present. With nonlinear stability analysis of amplifiers this technique can be re-employed. Here it is considered as a perturbation around a steady state AC operating point rather than a perturbation around a DC operating point. To do this, it is first necessary to apply an input signal which drives the amplifier into a known nonlinear state. Having established the working state, which will most likely be nonlinear for high efficiency power amplifiers then small signal PZ identification is conducted around this nonlinear operating point.

Unlike the DC stability analysis using PZ identification techniques which has a single DC operating point, the nonlinear stability analysis needs to be conducted at several drive conditions … in essence over the frequency-power level set {F1 … Fn, P1 … Pn} to ensure that the PA has been exercised or driven into as many operating states as is convenient. There is of course a trade off in terms of excessive simulation times and obtaining sufficient evidence of stability.

The analytical methods outlined in the introduction to pole zero analysis work only for small networks. For realistic circuits other PZ identification techniques need to be sought after. One such approach is to conduct a circuit analysis in the real frequency domain over a user specified range (which must not include the nonlinear drive frequency) and supply this data set to a network-system identification routine. Many math calculation packages come with identification routines that could be used, though these tend to be focused on the pure mathematical manipulations rather than the analysis of electronic circuits.

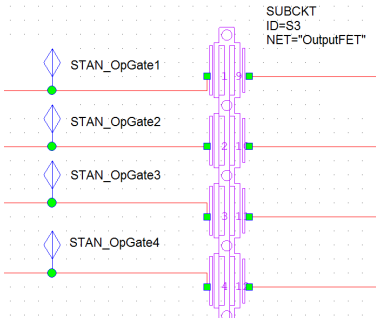
In the following example of the stability analysis of an MMIC amplifier the PZ identification tool STAN (AmCAD Engineering) will be used. This tool is part of AmCAD's IVCAD suite of tools. STAN needs to be provided a set of Z(jw) or Y(jw) data which can be set up in a parametric form when parameters such as drive power or element parameters need to swept.



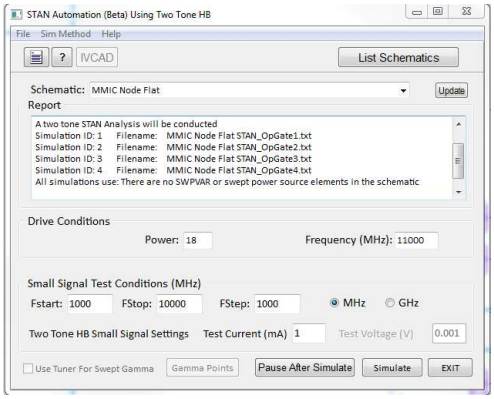


To assist in the creation of the data for STAN, we employ a wizard that is used to define bias, test nodes, create the measurements and store the STAN data. This wizard uses the AWRDE API making the stability analysis user inteface convenient and simple to use. Notice that the schematic is not populated with elements needed to define such an analysis. The only requirement here is for the designer to select wanted test nodes by placing the AWRDE element NCONN (named connector) at appropriate locations in the circuit and using the string 'STAN' in the NCONN's name. This process can work through schematic hierarchy if the amplifer is suitably complex.

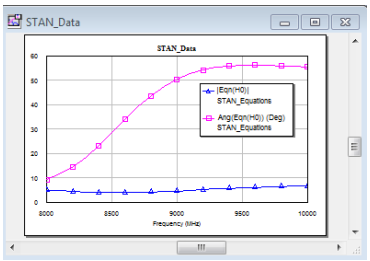
In the screen shot below one can see more clearly the nodes tested for stability analysis. These are automatically found by the wizard in packaging up the task of analysis and data collection which also creates separate files of data for use by STAN.



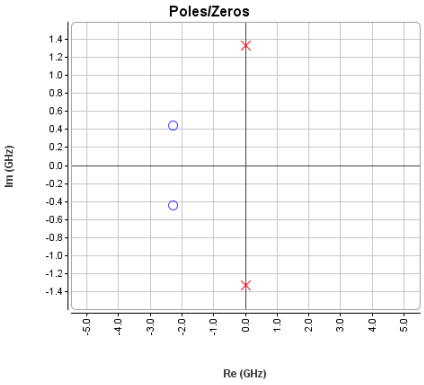
The wizard scans each schematic to see if it is appropriate for STAN analysis. This health check is performed to avoid errors in the preparation of robust STAN data.



The simulation process creates temporary graphs which in turn are used to provide the data for STAN analysis. These graphs can be viewed to see the suitability of the data, for example are there enough frequency points etc.



STAN's frequency domain identification techniques result in a PZ plot and a PZ table which can be exported to a spread sheet.



Type	Stability	Value Re	Value Im
Pole	Unstable	7405497.86008339	1.3257814881621847E9
Pole	Unstable	7405497.86008339	-1.3257814881621847E9
Zero	Stable	-2.288967721444612E9	4.4388427563554114E8
Zero	Stable	-2.288967721444612E9	-4.4388427563554114E8

In the example above one can see that the amplifier is unstable.

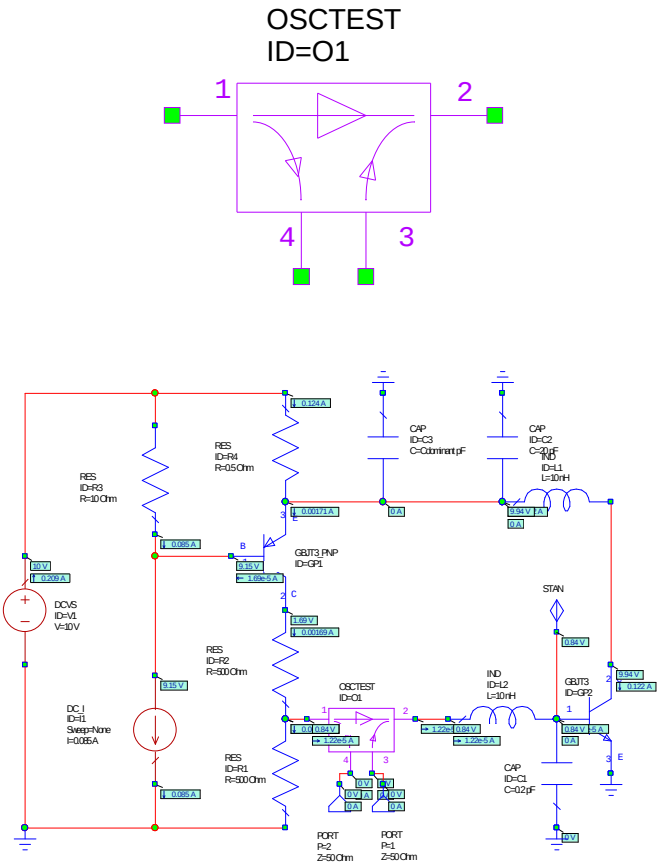
Using this information provided by the PZ identification process, the designer is then able to make decisions about which parameters need to be changed or what extra stabilizing elements need to be added to the network that guarantee stability without the sacrifice of amplifier performance. By doing multiple tests one can establish which nodes or loops are the most sensitive to changes that improve stability.

The unwanted generation of a simple sinusoidal waveform is only one type of manifestation of instability [3]. These range from noise bumps (also know as noisy precursors) seen in the spectrum around the wanted signal through to chaotic behaviour and multiple frequency quasi-static modes … and in extreme conditions period doubling. For frequency dividers, period doubling exhibited by varactor diodes under high drive conditions is of course desired.

In the case of HPAs, all these are unwanted phenomena. The noise bumps can be the most subtle, and unless care is taken to ensure that NF degradations beyond those associated with thermal noise have been properly assessed, it is possible that a HPA suffering form these effects can cause loss of system sensitivity.

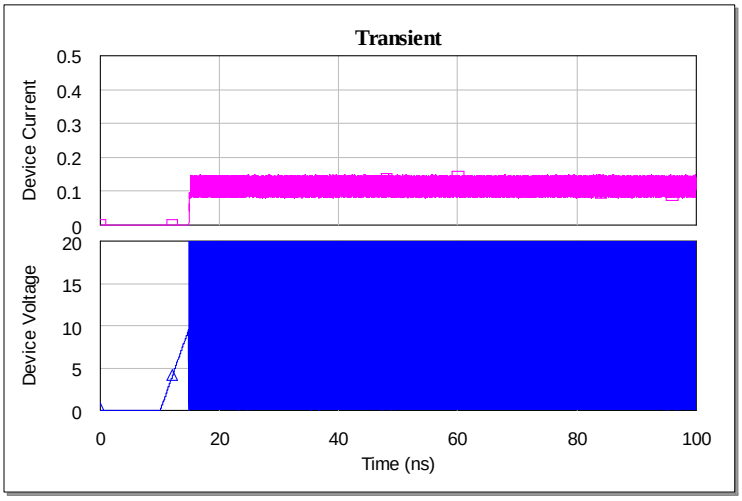
6. Complementary Stability Analysis Measurements

In the case of active bias circuits testing the negative feedback path is useful when loop gain and phase margins need to be assessed. The OSCTEST element can be inserted into a feedback loop at an appropriate position in the loop. This element is then used to conduct a small signal test by injecting a signal at Port 3 and measuring the resulting signal from Port 4 whilst maintaining the DC connectivity between Port 1 and Port 2.

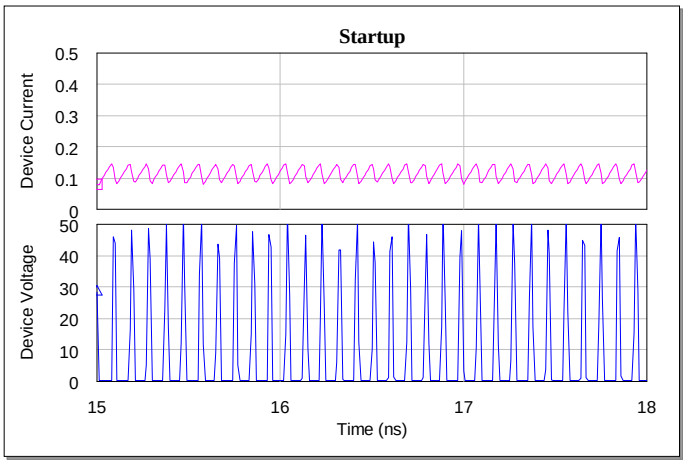


In this example, the OSCTEST element is being used to investigate the stability of the feedback circuit used to control the RF power transistor collector current. This current has been set to 122mA with a corresponding collector-emitter voltage of 9.94 volts. The low power bipolar PNP device controls the bias point of the RF PNP.

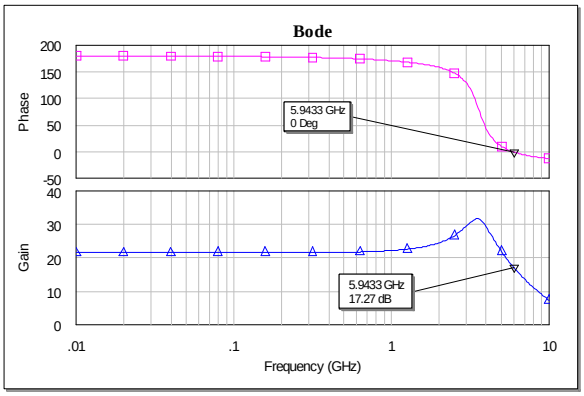
With the Cdominant capacitor set to 0pF the system is unstable. This can be seen by observing the transient behaviour of the system as the DC bias is applied. Please note that the scale selected for the voltage waveform graph truncates the peaks which are seen in the next illustration.



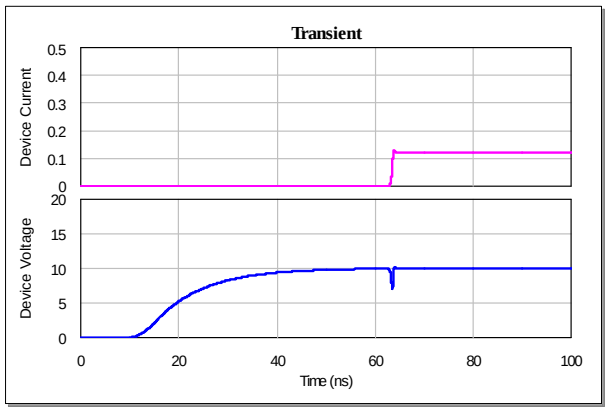
The device voltage and current are oscillating with a triangular waveform. The peak voltage may destroy the RF transistor.



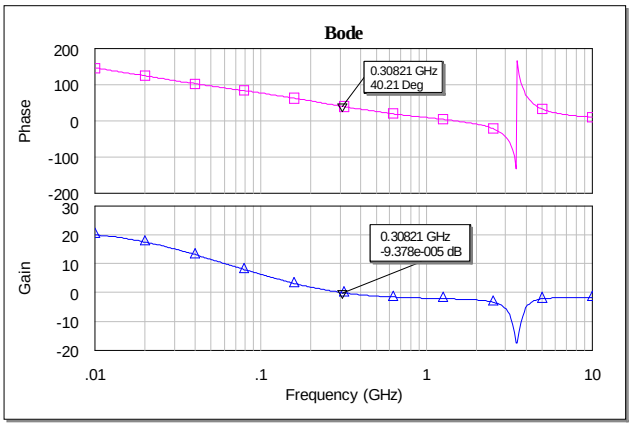
The loop gain and phase show that the system is unstable as the gain margin at 0 degrees phase shift is negative.



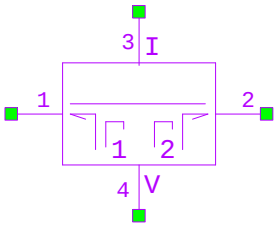
The classic application of a dominant pole to the system feedback path removes the oscillation. In the example circuit Cdominant = 20nF to ensure stability. The small kink in the collector voltage occurs when the RF transistor draws current.



The turn on process is now stable which is to be expected as the gain is now negative when the loop phase shift is zero. Another important aspect of this type of analysis is the exposure of potential problems. The inductive and capacitive elements may give rise to resonances, which coupled to high gain devices could threaten to reduce the stability margins. These elements are an inherent part of the RF bias circuitry. Not included in this diagram are the RF elements, matching and coupling needed for RF performance.

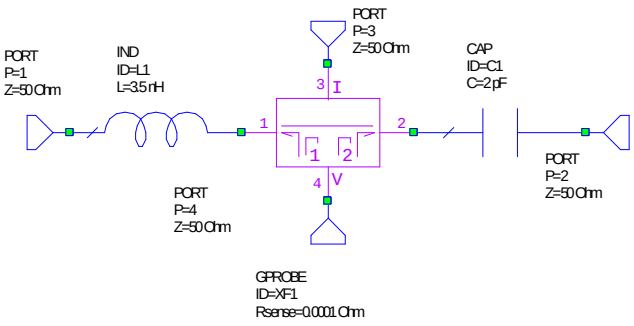


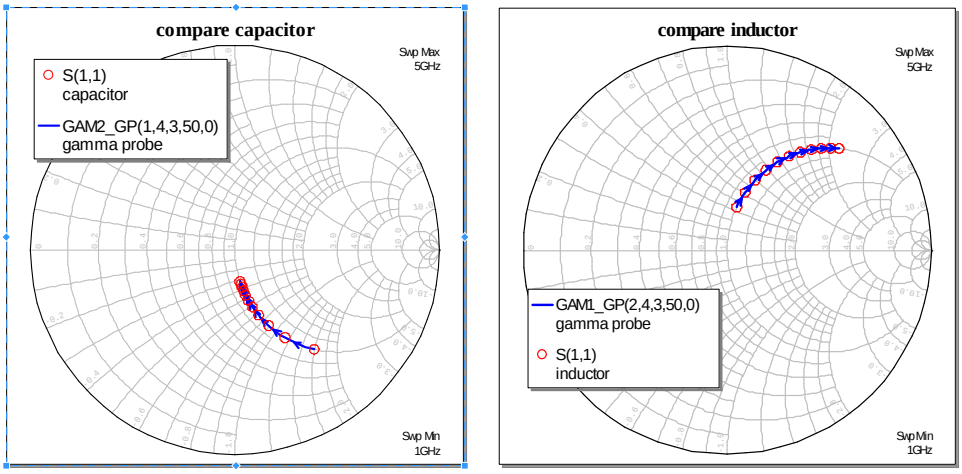
To complement the OSCTEST element the AWRDE has another test element called the gamma probe. This element is placed between circuit nodes and can be used to measure impedances.



GPROBE
ID=XF1
Rsense=0.0001 Ohm

The gamma probe is able to measure the impedance looking in the opposite direction from the source port. The simple schematic below illustrates the use of this element.





In the left hand side graph there are plots for the capacitive reactance of the capacitor in series with the terminal impedance (50 ohms in this case) measured directly in a test schematic (not shown) and by using the gamma probe. For completeness the measurement of an inductor is also shown.

This element uses two extra ports, the Voltage sample port and the Current sample port; these can be seen in the schematic above. One connection to the gamma probe will be labelled "V" and one will be labelled "I". The port hooked to the "V" connection should be the Voltage sample port and the port hooked to the "I" connection should be the Current sample port.

Conclusions

Modern design tools provide a comprehensive suite of utilities, test elements and analysis techniques for the assessment of stability analysis or circuits. These capabilities allow circuits to be investigated for potential stability problems under linear and nonlinear conditions. Their range and scope provides the engineer with the insights needed to investigate complex circuits, without which the verification of stability analysis would be tedious at best and unreliable or error prone at worst.

References:

[1] A. Platzker, W. Struble, and K. Hetzler, “Instabilities Diagnosis and the Role of K in the Microwave Circuits,” IEEE MTT-S International Micr
owave Symposium Digest, pp. 1185–1188, 1993.

[2] Kuo, “Network Analysis and Synthesis”, Wiley.

[3] A. Suarez and R. Quere, Stability Analysis of Nonlinear Microwave Circuits, Artech House, Norwood, MA, 1993.