Custom MMIC Packaging Solutions for High Frequency Thermally Efficient Surface Mount Applications.

Steve Melvin
Principal Engineer

Teledyne-Labtech
8 Vincent Avenue, Crownhill, Milton Keynes, MK8 0AB
Tel +44 1908267611

smelvin@teledyne.com

ABSTRACT

Microwave printed circuit board processing can be used to produce MMIC packages with excellent RF and thermal performance. In the drive to reduce manufacturing complexity and thereby cost, microwave system manufacturers are designing products to use standard surface mount assembly. However the elimination of the 'chip and wire' assembly stage does not remove the need for high frequency interconnects or for good RF grounds. Similarly, MMICs that have high power dissipation still require good thermal mounting. Relatively simple packages made from 100um LCP offer a MMIC packaging solution that can be used within a standard surface mount assembly facility.

INTRODUCTION

MMIC packages have traditionally been designed as drop-in circuits such as that shown in figure 1, and these still form an important technology especially for high power devices. The circuit can be made as a pre or post bonded assembly and by virtue of the solid metal carrier has excellent thermal performance.

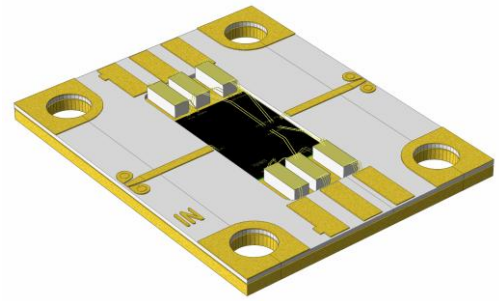
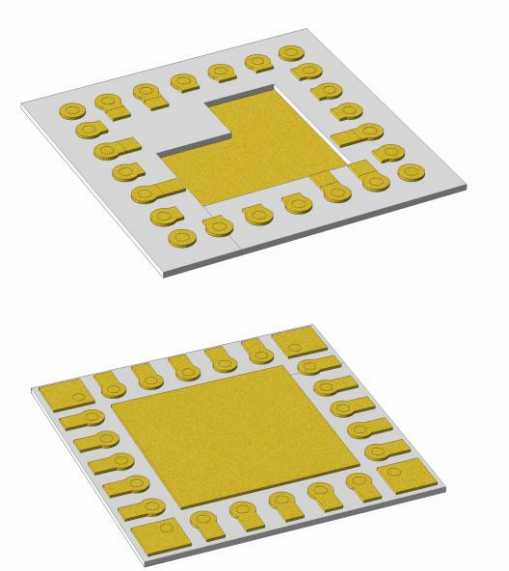


Figure 1

For surface mounted applications a package can be formed from typically a Rogers RO4000 series laminate or more recently ULTRLAM 3000, referred to here as LCP. The mechanically machined RO4000 series packages are excellent for lower frequency and large scale packages, but with laser machining the LCP material can be used to make packages that are similar to plastic QFNs but with superior high frequency performance.

PACKAGE DESIGN

With 100um LCP as the dielectric material, laser formed holes and pockets can be used with the appropriate plating to fashion a MMIC package that is patterned on both sides and has via connections from the top to bottom surface. The removal of the dielectric exposes the upper surface of the bottom copper layer which is subsequently plated; this is used as the mounting surface for the MMIC. This bottom layer is a sandwich of copper, nickel and copper, the nickel is used as a stiffener and the final thickness of the lower plated sandwich is around 90um. A typical 5x5mm package is shown in figure 2. In this example the laser cut pocket is cut to allow 50um around the MMIC and the cavity is shaped to accommodate a decoupling capacitor to be mounted close to the MMIC. The top copper circuit can run up to 50um from the pocket edge. These short distances coupled with the 100um dielectric thickness allow wire bonds to be kept short where necessary.



Figures 2A and 2B

The final plating can be thick gold for low loss applications but is generally the 'Universal Finish.' This plating scheme has 3-6um of nickel on the 45um thick copper circuit, with a further plating of 0.2-0.5um of palladium and a final layer of 0.005um of gold. This provides a good stable finish for wire bonding and soldering.

INSERTION LOSS

The 'Universal Finish' uses both nickel and palladium, neither of which is particularly good for low loss transmission lines, although the transmission line lengths in MMIC packages are generally short. To accurately model the losses a multi-level EM simulation was carried out with EMSight.

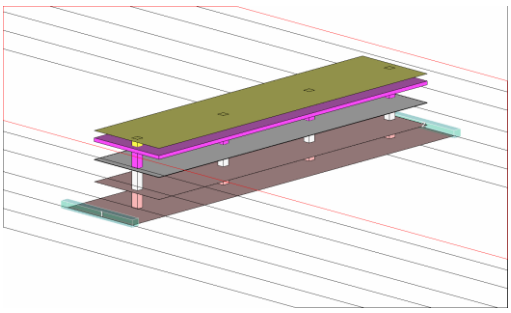


Figure 3

Figure 3 shows a 3D view of the metal layers in a simulation for a 1mm line. The bottom copper layer is modelled as two layers and the conductivity is halved for each layer. The metals are connected through separate air layers set to the metal thicknesses. The EM grid was set to have 12 square cells across the line as this has been found in previous work to quite closely model a very dense grid. In order to speed up simulation times for subsequent circuit designs a simpler 2 layer model was set up and the conductivity adjusted until the performance of the 2 layer system matched that of the four layer one. The predicted performance of the lines is shown in figure 4. The line loss is around 0.035dB/mm at 40GHz.

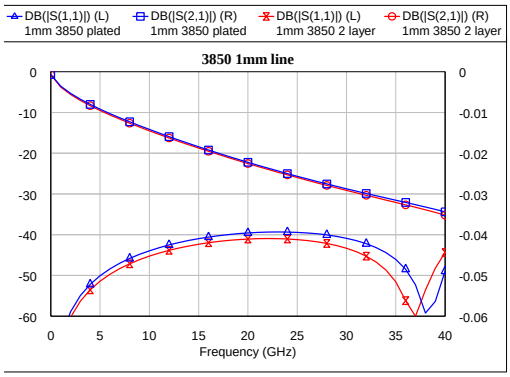


Figure 4

PACKAGE TRANSITION

With the 2 layer metal system and realistic simulation times the RF through connection was designed. The thick metal simulation is used as the plated metals are similar in height to the substrates and the spacing between the metals is similar to their thicknesses and this method models the increased coupling between the metal faces. Figure 5 below shows a 3D view for a 100um LCP plated through hole on a 203um RO4003 circuit in a QFN style footprint.

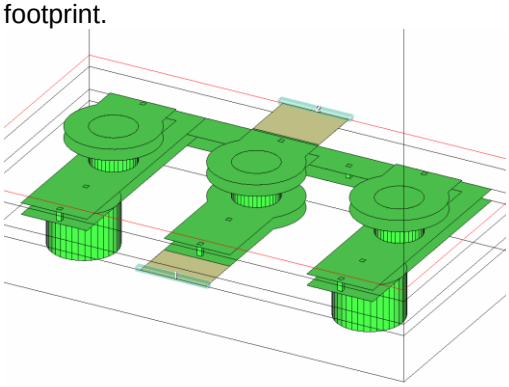


Figure 5

The overall performance is a combination of the package and its motherboard and is summarised in figure 6 below. The insertion loss is near 0.15dB

at 40GHz but this includes a reflected component from s11 and s22. A better gauge of the true loss is Gmax at -0.07dB.

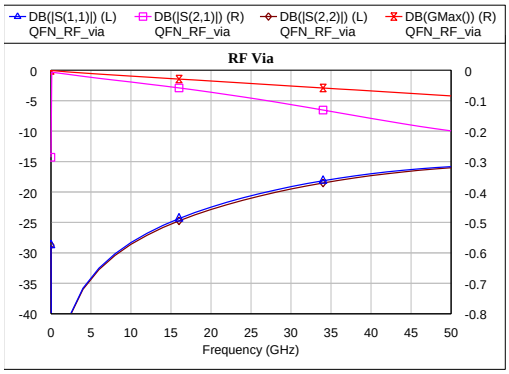


Figure 6

The RF via is resonant free to 50GHz as there is a ground connection at both ends of the traces on either side of the centre conductor. Leaving either end open circuit results in a resonance at about 38GHz. This can be seen in the measured results (Figure 7, red trace) for a similar 5x5mm package with no connection to the under package ground. This can be predicted in the EMSight analysis and is shown in blue.

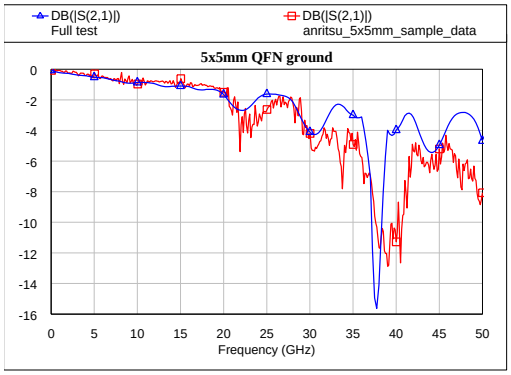


Figure 7

MEASURED RESULTS

Figure 8 shows the insertion loss and input return loss for a 5x5mm QFN style LCP package mounted on a 203um thick RO4003 test board. The QFN has a through line patterned on the upper surface with no pocket. The red data is the measured performance; the blue is the predicted performance for the same assembly. Comparing the Gmax for a 70mm RO4003 through line with the Gmax for the test board and 5x5mm QFN gives around 1dB difference in the loss which is attributable to the package, see figure 9.

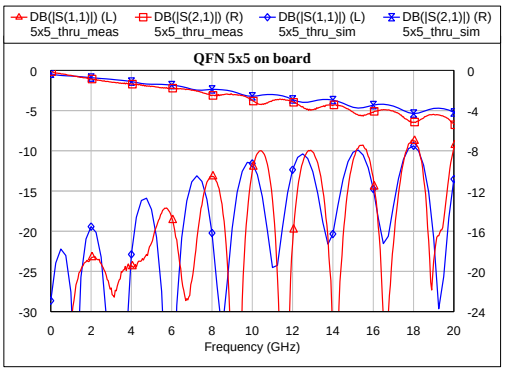


Figure 8

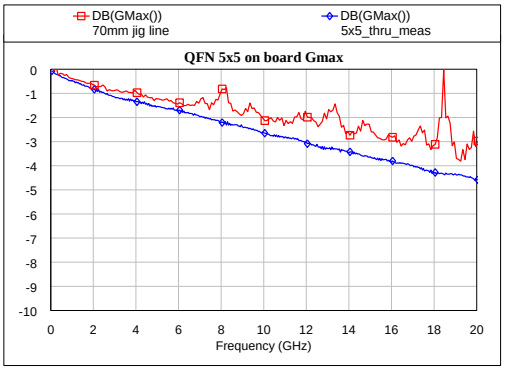


Figure 9

The simulation under predicts the insertion loss in figure 8. This is probably due to the simulation for the RF transition not including the loss resulting from currents in the z-axis. EMSight does not solve for loss in the z-axis and better accuracy would need a full 3D analysis. However the difference between the test jig line and the mounted package shown in figure 9 shows the package to have around 1dB loss. With a MMIC fitted the through line loss would be removed and the loss for each RF transition would be under 0.5dB.

ISOLATION

Teledyne-Labtech manufactures an extensive range of PIN diode switches. Off-state isolation is a key performance parameter for these devices and they are normally sealed in channelised aluminium housings to meet this requirement. The MMIC packaging technology has been applied to the PIN diode SPDT shown in figure 10 made using the 100um LCP process. Without any amplifier gain it better facilitates assessment of the package isolation.

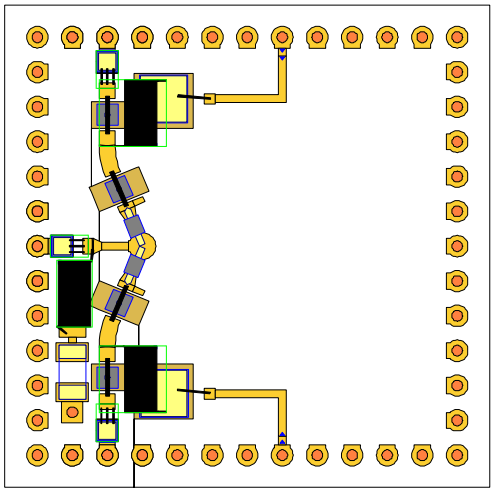


Figure 10

Figure 11 shows the measured isolation for a 9x9mm 44 pin QFN style package. The package is similar to that for the PIN switch shown in figure 10 but has the vias on four sides and no other traces on the upper surface.

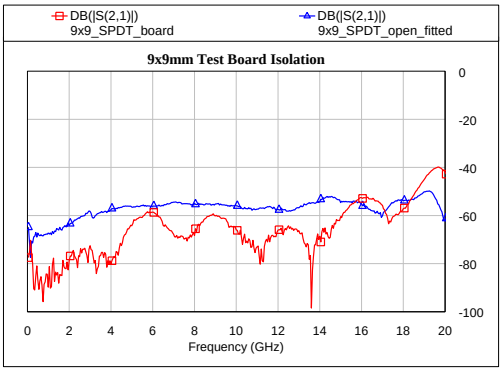


Figure 11

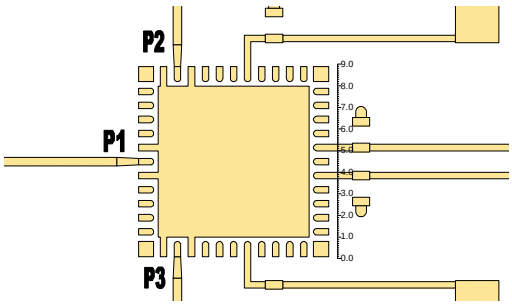


Figure 12

The measurement is not stripped and includes 3dB per port of insertion loss at 40GHz. The red trace shows the insertion loss for the test board only (figure 12) and the blue trace shows the insertion loss with the empty QFN package fitted. The measurements show a good level of isolation and that the fitting of the package has only a small effect over a wide frequency range.

For completeness the measured off state isolation for the fully assembled switch is compared with that for the empty LCP circuit. Figure 13 has the empty package in blue and the fully assembled switch in pink. As can be seen the isolation of the switch, normally >70dB at 10GHz, is reduced to that of the package and mounting.

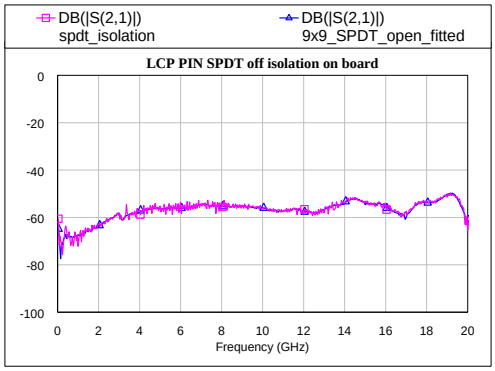


Figure 13

Whilst the port to port isolation might be very good for the package, it is often the environment that dominates the isolation of the fitted assembled part. Any metallic cover used to form a waveguide cut-off channel above the package will be limited by the package width. The graph in figure 14 shows the evanescent mode attenuation in a waveguide the effect of the dielectric of the MMIC package in the waveguide is to lower the cut-off frequency. At 10GHz a 10mm cavity to cover the 9x9mm SPDT would only provide 2dB/mm of attenuation.

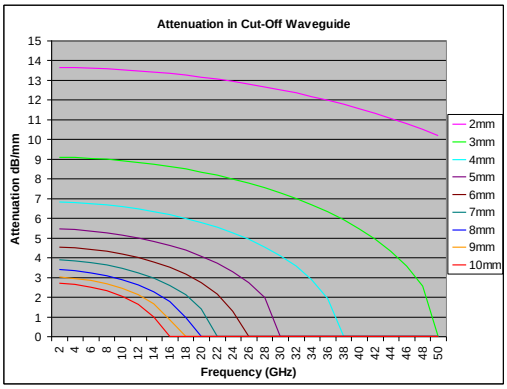


Figure 14

THERMAL CONSIDERATIONS

There are two aspects to the thermal performance of the assembled and mounted MMIC package, firstly the plated metals of the underside of the package that is the MMIC mounting area, RF ground and low thermal resistance connection, secondly the motherboard mounting area.

PACKAGE BASE

The 5x5mm package in the earlier example has a central 3x3mm plated metal base that forms both the RF ground and a low thermal resistance path for the dissipated device power. The 90um thick copper-nickel-copper sandwich of the base is plated on both sides with the 'Universal Finish'. This gives a 100um thick 9 metal layer column as the ground connection. Table 1 summarises the layer thicknesses and thermal resistances.

The overall thermal resistance for the 3x3mm ground pad is near 0.056°C/W. However this assumes heat flowing as a column through the whole package base. A more accurate analysis would use the active device dimensions and assume a 45° spreading angle. A 1x1mm heat source would have a thermal resistance path of more like 0.5°C/W.

Metal	W/m/K	Height mm	Rth °C/W
Au	310	0.00005	0.00002
Pd	71.8	0.00040	0.00062
Ni	91	0.00450	0.00549
Cu	401	0.03500	0.00970
Ni	91	0.02000	0.02442
Cu	401	0.03500	0.00970
Ni	91	0.00450	0.00549
Pd	71.8	0.00040	0.00062
Au	310	0.00005	0.00002
Totals		0.0999	0.05608

Table 1

MOTHERBOARD

The mounting area on the motherboard provides the next thermal connection in the path to a good heatsink. There are two main considerations in the design of this contact area. The first is ensuring a good a resonance free ground connection for the MMIC, the second is providing a low thermal resistance path.

The ground pad under the MMIC is important as it can be source of spurious RF performance. Oscillations in otherwise stable MMIC amplifiers and sharp dips and spikes in the gain versus frequency characteristic are known problems. The problem arises as the finite impedance of the interconnecting vias holds the ground pad potential above that of true ground. Figure 15 shows the insertion loss for a ground pad that has different numbers of 0.3mm diameter via connections from the pad to the ground plane. The blue trace shows the effect of just four via connections as shown in figure 16a; the red trace is for 13 vias in figure 16b, with 25 vias in brown for figure 16c.

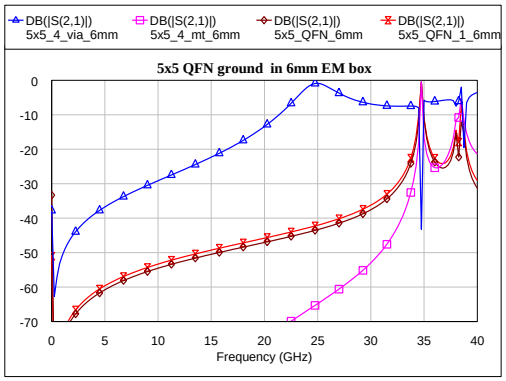


Figure 15

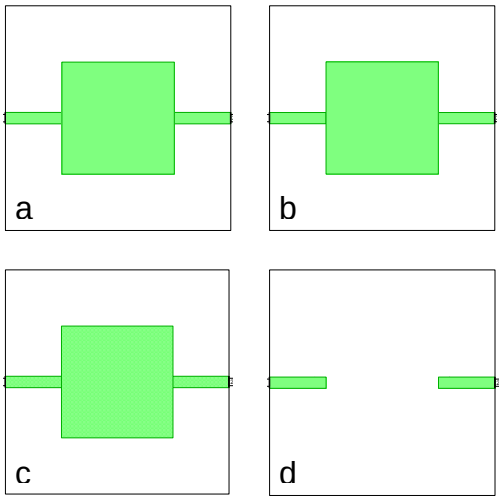


Figure 16

The blue trace shows the insertion loss falling to a low value at 25GHz, with the feed traces connected directly to the ground pad this shows a high impedance in the RF ground connection. The ground pad can be made to have a lower impedance by the additional vias in b and c.

The spikes shown in all three traces above 34GHz are not a product of the ground connection, as the pink trace shows the insertion loss for just the feed lines minus the ground pad, figure 16d.

The thermal resistance of the ground pad is a combination of the heat path through the mounting area metal and substrate and the path through the metal via connections to the ground plane. For the 3x3mm example above the thermal resistance of the ground pad alone is 33°C/W. Each via is a metal tube 300um in diameter, 203um long with sides formed from 30um of plated copper. Assuming no heat is lost through the side walls of the via into the substrate the thermal resistance of each via is 19.9°C/W. With the 25 vias in the motherboard ground pad in figure 16c the combined thermal resistance is approximately 0.8°C/W. This is useful as a guide as it assumes the heat source is spread evenly over the base of the MMIC package. A more accurate analysis would need a 3D model of the assembly.

Filling the via holes with conductive epoxy is only moderately successful in lowering the thermal resistance of the motherboard ground. Using Diemat 6030HK as the filler lowers the via thermal resistance to 15.7°C/W and the motherboard thermal resistance to 0.63°C/W for the example in figure 16c. Using a standard silver epoxy with a thermal conductivity of 4W/m/K the reduction is to only 19.5°C/W per via.

SUMMARY

Simple MMIC packages in 100um LCP can be optimised easily for single chip or multi-chip applications. The simulated and measured results show low insertion losses and good levels of isolation. The simulation of the plated metals can be simplified to a two metal layer system enabling a time efficient 2.5D solution for the RF transition. The simple construction allows a low impedance microwave ground connection for the MMIC that doubles as a low thermal resistance path for the dissipated power.

REFERENCES

Microstrip Conductor Loss Models for Electromagnetic Analysis. James C. Rautio*, Fellow, IEEE,* and Veysel Demir*, Student Member, IEEE,* IEEE Transactions on Microwave Theory and Techniques. Vol 51, No 3, March 2003

Connecting MMIC Chips to Ground in a Microstrip Environment. Swanson, Baker and O'Mahoney. Microwave Journal December 1993.