The Application of the Cardiff Look-Up Table Model to the Design of MMIC Power Amplifiers

D. M. FitzPatrick [(1)], S. Woodington[(2)], J. Lees [(2)], J. Benedikt[(2)], S.C. Cripps [(2)], P. J. Tasker[(2)]

[(1)] PoweRFul Microwave, 15 Adelaide Place, Ryde, Isle of Wight, PO33 3DP,
www.powerfulmicrowave.co.uk

[(2)] Centre for High Frequency Engineering, School of Engineering, Cardiff University, Cardiff, CF24 3AA, Wales, UK

Abstract

The design of microwave power amplifiers has been greatly enhanced by the use of CAD; however despite the improvements in the area of E-M simulation and non-linear analysis, designs still often require to be 'tweaked'. While this may be a practical option for discrete amplifiers it is extremely difficult in the MMIC domain. The requirement for increased efficiency operation and hence the use of modes such as class F and J have highlighted inadequacies in current models. This paper describes the use of waveform engineering not only in the area of device measurement, but also as an integral part of the MMIC design process. The practical limits on current nonlinear models are discussed and an example design using harmonic enhancement, is shown.

Introduction

In a previous paper [1] a measurement system for the characterisation of passive and active microwave devices was described. This system has been used to collect data on the performance of microwave transistors at X band and to analyse their performance in impedance environments presented by matching circuits designed to optimise device performance. The motivation for this work has been driven by the desire to produce amplifiers with the highest possible efficiencies and the need to address some of the inadequacies in the existing design process, which result in extended design cycles due to the need to iterate circuits and wasted wafer 'real estate' from multiple iterations.

In order for device foundries to produce models the process must be, if not at the final production release stage, at least fairly close to it. Thus there is a time lag between the release of a production process and its usability by the industry – waiting for availability of nonlinear models. The creation of device models supplied by foundries consist of the fitting of a complicated circuit model (the TOM3 model has over 100 elements) to a set of specific measurements, details of which are not always available to the design engineer. Hence designers will use a model with which they have confidence from previous experience or at least with which they are aware of the limitations. This may thus restrict them to using, for example, non optimum bias settings for their particular application. Alternatively models are used to get a design 'in the right ballpark', and multiple iterations are laid out and the one giving the best performance is chosen. Either way there is a requirement to have performed some characterization of the transistor [2]. The suggestion of this work is that these confidence building measurements instead be used to create a model for the specific conditions which suit the particular design requirement and then test the performance within the anticipated environment.

One of the key advantages of the Active Load-Pull measurement System (ALPS) at Cardiff University [3] and its suitability to

characterization of high frequency devices, (including harmonic load-pull), is that it can overcome the system losses and produce high reflection coefficients. Conventional passive load-pull systems struggle at these high frequencies due to loss and bandwidth limitations. Using this system the optimum impedance environment can be determined for maximum performance under particular operating conditions [4].

The benefit of integrating the ALPS into the design process is that data used is fully representative of the real device performance. The measurement data is stored in a Direct Look-Up Table (DLUT) model, which can be added to as more data is collected. Models for passive structures are relatively well defined and the addition of Electro-Magnetic (E-M) simulation means that the performance of matching structures can be close to predictions.

Overview of the Design Process

The proposed design process is summarised in the steps outlined in figure 1. The measurement activity is linked in with the CAD so that as new circuit matching networks are produced their impact on device performance can be evaluated. Thus the designer is confident as to the actual performance that will be achieved when the circuit is manufactured.

The device is first measured either across a large part of the impedance plane or targeting specific regions based on theoretical behaviour [5]. The effects of bias and power level can be examined so that the optimum levels can be used for the application. When mapping large areas the harmonic impedances are held at a specific known value, typically 50Ω. If a particular operating mode is being created (such as class F) [6] then the harmonics are held at the relevant magnitude and phase.

To create the DLUT model a measurement grid is established across the load plane and at each point on the grid the power is swept so that the device is driven to a level where the output power is about 3 dB into compression.

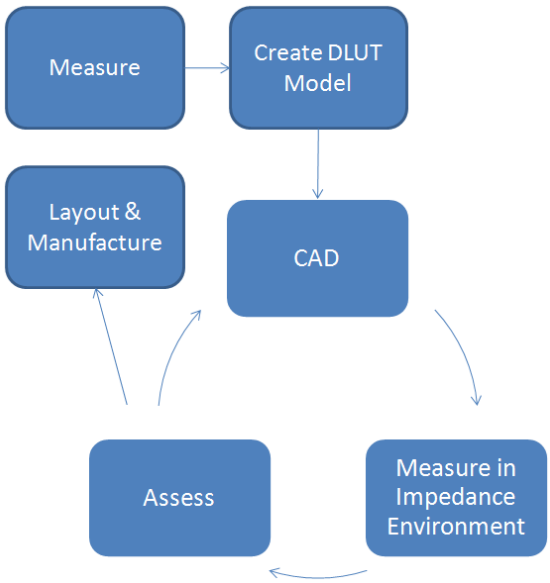

Figure 1: Flow of Design Process

The incident and reflected voltage and currents at both terminals of the device are measured and the characteristics of the device (gain, power, efficiency, match, etc.) calculated. A DLUT model is created using the industry standard MDIF (Measurement Data Interchange Format). This file contains the data for each load impedance point, referenced to the input voltage [7]. The data file can be imported into a non-linear simulator for analysis. Note however that any such analysis will only be accurate within the boundaries of the data acquired. Changing the operating conditions (bias, impedance etc.) will result in a potentially inaccurate simulation. If operation with a different set of conditions is required the measurement loop is repeated and these additional data points added to the model file.

When an adequate data set has been obtained the matching circuits can be developed in the normal way. These are likely to include harmonic impedances that were not in the original MDIF file. Thus it is important to return to the measurement system and terminate the device not only with the calculated fundamental load, but also with the expected harmonic impedances [8]. Again, this new data can be added to the

MDIF file. This loop is repeated until satisfactory performance is achieved from the device in the simulated and measured load impedance environment.

Model Accuracy

An analysis was conducted using data acquired in the first stage of the design process to assess the accuracy of the DLUT and compare it with the performance of the non-linear model contained within the Process Design Kit (PDK) of the foundry. The model was analysed with the load impedance corresponding to the maximum for Power Added Efficiency (PAE), table 1.

GaAs pHEMT 10x75 at 9v 150 mA measured at 6 GHz at an input power level of 18.6 dBm			
Maximums	Value	Γ mag	Γ pha (°)
PAE (%)	51.4	0.35	65.9
Pout (dBm)	28.0	0.22	78.1
Gain (dB)	16.4	0.61	94.3
Drain Eff. (%)	53.0	0.35	65.9
Table 1. Maximum performance values and corresponding load impedances			

The measured results were compared with that of the DLUT and the PDK as shown in figures 2-3. It should be noted that the PDK model is a 'best fit' over a wide variety of bias conditions, power levels and device sizes. Thus it cannot be expected to exactly replicate actual performance in all instances. As can be seen, in these cases it accurately simulates the fundamental output power over the measurement range. It is however consistently optimistic with regards to efficiency calculations and measurements of the 2nd and 3rd harmonic levels differ. The DLUT model in contrast is consistent with the measurements. It should be noted that whilst the measurements were in 1dB steps of drive power the analysis was in 0.1 dB steps, confirming the interpolation of the DLUT model with input power. Investigating the harmonic performance further, a load pull of the 2nd harmonic across the entire impedance plane was conducted, figure 4, and compared with the same measurement carried out in the simulator of the PDK model.

It was noticeable that not only was the PAE variation half as much in the PDK model, but also that the phase was rotated by ~180°.

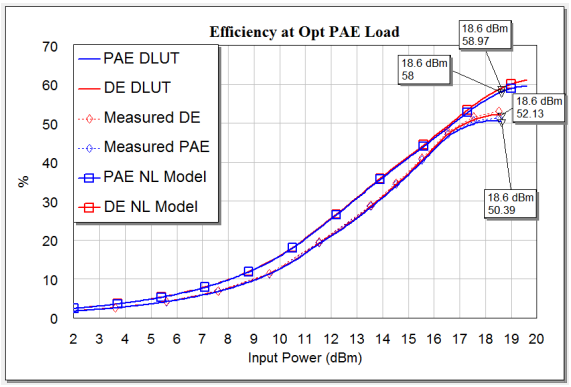

Figure 2: Comparison of PAE performance of measured data, DLUT and PDK nonlinear models at optimum PAE load.

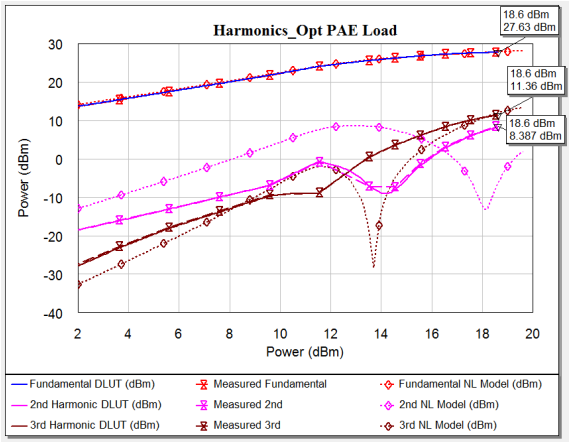

Figure 3: Comparison of Fundamental and harmonic levels between measured data, DLUT and PDK nonlinear models at optimum PAE load.

The effect of the 2nd harmonic impedance shown in figure 4, points the designer at the areas of the impedance plane to be targeted (and to be avoided) to maximise the PAE of the device, as will be discussed in the next section.

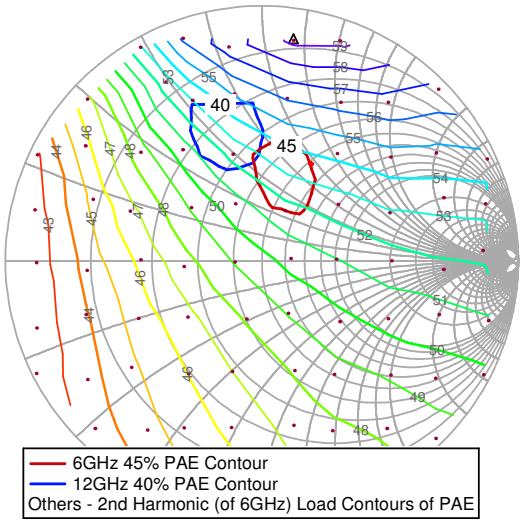

Figure 4: Effect 2nd harmonic load pull across the full impedance plane. PAE variation >16%.

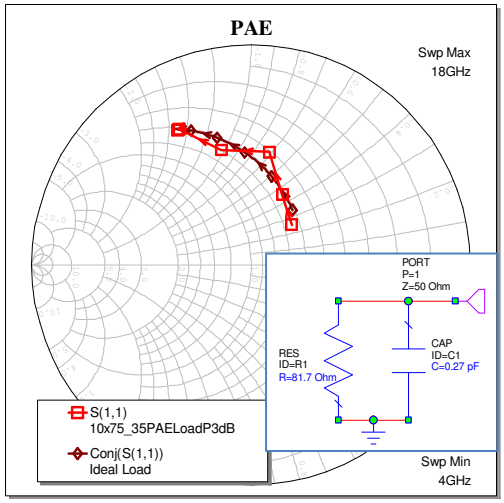

Figure 5. Measured Optimum PAE Load points and conjugate match to by simple equivalent device output circuit.

Design Example

To demonstrate the operation of this methodology the output matching network of a 5-10 GHz ½W driver stage was designed, using harmonic enhancement at 6GHz to maximise PAE. An equivalent circuit to the optimum PAE fundamental loads (table 2), from measurement data was created and the conjugate impedance of this circuit plotted on a Smith Chart as the target load trajectory, figure 5.

Freq. (GHz)	Γ_L (Mag/Ang)	PAE (%)	Pout (dBm)	Gain (dB)
4	0.26/44.6°	49.2	27.4	21.1
6	0.35/65.9°	51.4	27.7	15.0
8	0.52/80.8°	51.2	27.0	13.5
12	0.54/104.1°	44.5	27.2	10.8
16	0.70/118.0°	36.6	26.2	9.7
18	0.70/118.6°	35.1	26.0	8.1

Table 2, Measured optimum PAE loads and associated performance.

Note that as the optimum impedances follow a constant admittance curve it is possible to take measurements at fewer frequencies to establish the required impedances over a wide bandwidth.

In this case we wish to maximise the PAE at 6GHz, which can be achieved by optimising the termination of the 2nd harmonic [8]. Rather than target a specific load at 12 GHz, a region of the impedance plane is chosen, and a circuit topology which will both produce the fundamental load impedances and the 'steering' of the harmonic is selected. Initially idealised elements are used as shown in figure 6 and the performance is shown in figure 7, (green trace).

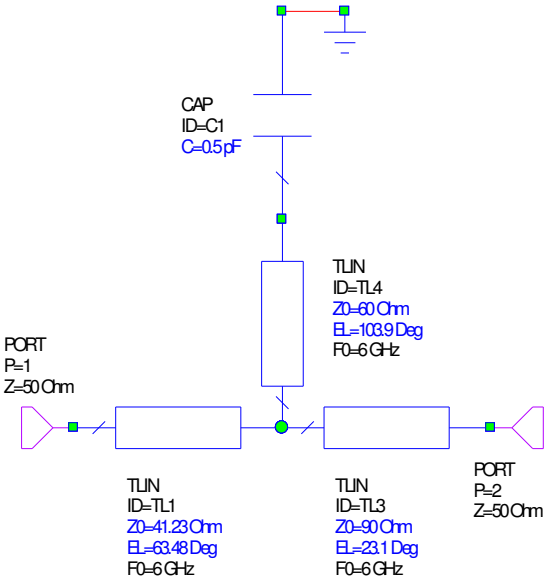

Figure 6: Idealised matching section providing 5-10 GHz optimum PAE match and 6 GHz 2nd harmonic enhancement.

The idealised elements are replaced with physical models for the transmission lines and decoupling capacitor and the circuit re-optimised (figure 7, blue trace). At each stage the device in the measurement system is analysed with the predicted fundamental

and harmonic load impedances, to check the performance is still satisfactory.

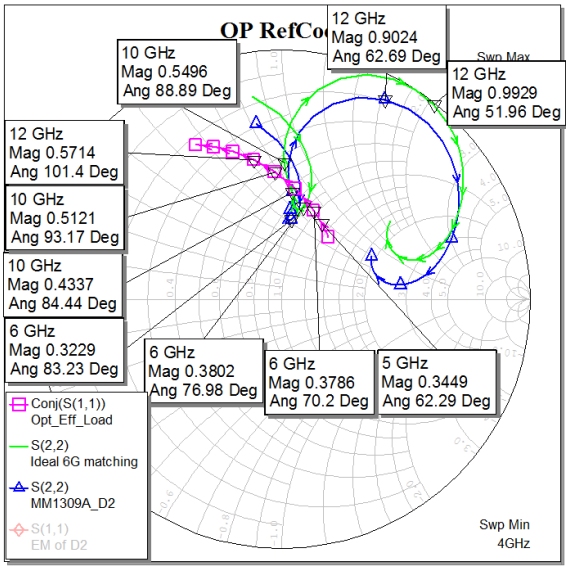

Figure 7: Optimum, ideal and physical matching circuit impedances.

The stage is then laid out within the constraints of the available area for the test cell. No input matching was included in this design due to limits on circuit area available and also the desire to make the most accurate comparison between individual device and output matched device on the same wafer, (input matching circuits could be de-embedded but this adds a layer of complexity and source of uncertainty).

The wafer cell is shown in figure 8 and includes, de-embedding structure, individual transistor, separate output matching circuit and finally the combination of device and output matching.

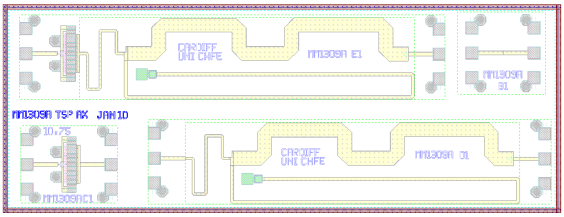

Figure 8: CAD layout of MMIC and test structures.

The matching circuit was analysed using linear and E-M simulators, which gave differing results particularly as frequency increased. The E-M analysis included passive elements from the PDK for capacitors and via holes. Analysis shows that predictions for load impedance vary between the two simulation methods, these are summarised in table 3.

Target Load Impedances	Fundamental, Γ_1 (Mag/Ang)	2nd Harmonic, Γ_2 (Mag/Ang)
From linear simulation	0.32 /_ 83.2°	0.90 /_ 62.7°
From EM simulation	0.32 /_ 98.0°	0.96 /_70.0°

Table 3, Match results at 6 GHz from linear and E-M analysis.

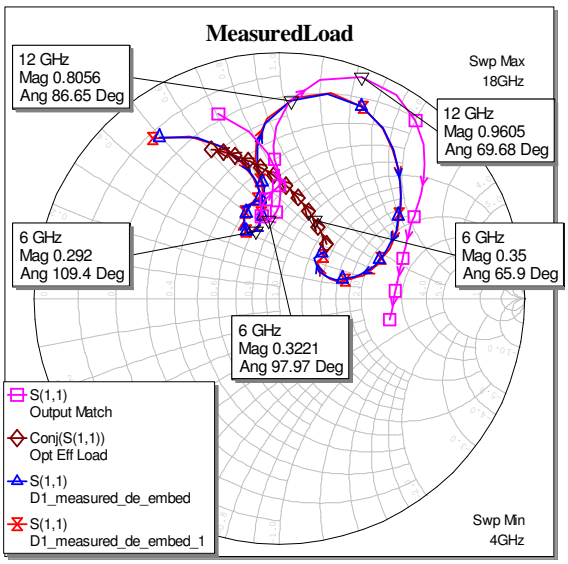

Figure 9: E-M predicted impedance and measured load impedances of the de-embedded output matching circuit.

The manufactured MMIC and the separate output matching circuit were tested. The actual load presented to the device by this network at the fundamental frequency was 0.29/_109°, and at the 2nd harmonic, 0.81/_87°. The performance of the original device and the measured circuit is summarised in table 4. The measured results from the manufactured MMIC include the losses of the output matching circuit. These can be removed by de-embedding to make a true comparison with the single device, (bottom row, table 4.).

It can be seen from the results of table 4 that the device measured at 6 GHz achieves greater than the target ½W of output power and with a PAE >49%.

One of the problems with the DLUT model is that for accurate simulation, for

each fundamental load point the area of possible harmonic loads (at least for the 2nd and probably the 3rd depending on the degree of accuracy required) need to be measured and stored. Add to this input power sweeps and the data array becomes very large. A further issue is that the simulation relies upon historic data, i.e. the performance of the original measured device. For this reason an individual device is included in the layout so that its performance can be compared to that of the unit used in the design. As a history is built up on typical device models a picture of expected yield can be created.

Γ_1 Mag/ Ang	Γ_2 Mag/ Ang	Pin (dBm)	Pout (dBm)	MAG (dB)	PAE (%)
0.43 /_70°	0.90 /_71°	13.4	27.7	14.3	61.5
0.29 /_109°	0.81 /_87°	16.1	28.1	12.0	49.0
0.29 /_109°	0.81 /_87°	16.1	28.8	12.7	58.2

Table 4, Measured performance at 6 GHz of device with load reflection coefficients from, E-M analysis (top), measured MMIC (middle) and MMIC de-embedded to device (bottom).

In this case measurement of the device manufactured on the MMIC wafer run showed an increase in performance over the original device used in the design, as shown in table 5, hence the better than anticipated performance.

We can also see from table 5 that the output matching circuit has provided improvement to the PAE. The maximum PAE with the optimum load is 55.1%, however the actual load presented was some way from this and should have given a PAE of 44.0%. From table 4 it can be seen that the PAE at the output of the device is 58.2%, a marked improvement.

Parameter	Original Device	New Device
Opt PAE load	0.35/_66°	0.43/_70°
Pin (dBm)	12.6	12.9
PAE (%)	51.4	55.1
Pout (dBm)	27.7	27.5
DE (%)	53.0	57.1
MAG (dB)	15.0	14.6

Table 5, performance at optimum PAE for the two device runs.

Conclusions and future work

A process has been demonstrated that gives MMIC PA designers better insight into the operation of high frequency transistors in a user defined environment, as opposed to that prescribed by historical data or foundry modelling. It has been shown how this nonlinear information can be utilised within existing CAD software so that reliable circuit topologies may be derived with a high degree of confidence in achieving performance targets in manufacture.

The model used has been shown to have excellent agreement with measured performance within the envelope of the test conditions. The model can be added to as more measurements are taken.

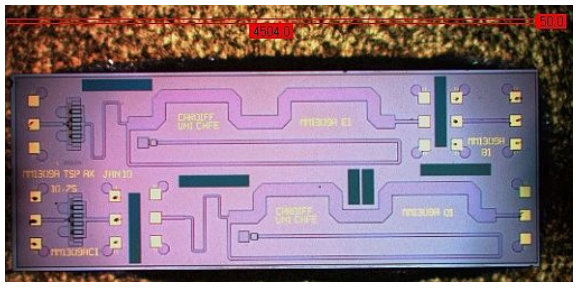

Figure 10: Manufactured MMIC and test structures.

Further work on the modelling approach is looking towards replacing the measured data grid with polynomial coefficients which describe the power waves as a function of load impedance and input drive. This will not only greatly reduce the size of

the data table, but also reduce the relative number of measurement points required as only sufficient points to describe an ellipse are needed, thus increasing the practicality of conducting measurements over power ranges, fundament loads and harmonic loads.

Acknowledgments

The work reported in this paper was funded by the Electro-Magnetic Remote Sensing (EMRS) Defence Technology Centre, established by the UK Ministry of Defence and supported by SELEX Galileo. Thanks must also go to Malcolm Edwards and Taisto Tinttunen of AWR for their help in implementing the Cardiff DLUT model in Microwave Office.

References

1. D. FitzPatrick, T. Williams, "High Frequency Sampling Technique for Microwave Active and Passive Device Characterisation", ARMMS Nov. 2007, Rockingham.
2. C.Schuberth, H. Arthaber, M. L. Mayer, G. Magerl, R. Quay and F. van Raay, "Load Pull Characterisation of GaN/AlGaN HEMTs," International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits, pages 180-182, January 2006ac, *Wireless sensor network designs*: John Wiley & Sons, 2003.
3. T. V. Williams, D. FitzPatrick, M. Haynes, C. Whittle, J. Benedikt and P. J. Tasker, "A High Frequency Time Domain Measurement System and its Application to Robust and Scientific Ultra-Wide Band MMIC design for Military Applications", 5th EMRS DTC Technical Conference, Edinburgh, 2008.
4. D. M. FitzPatrick, J. Lees, A. Sheikh, J. Benedikt, P. J. Tasker and T. Williams, "Fundamental & Harmonic Termination Impedance Considerations in the Design of Optimally Efficient Wideband MMIC PAs", 6th EMRS DTC Technical Conference, Edinburgh, 2009.
5. S.C. Cripps, "RF Power Amplifiers for Wireless Communications", Artech House, London, 2006.
6. P. Wright, A. Sheikh, C. Roff., et. al. "Highly efficient operation modes in GaN power transistors delivering upwards of 81% efficiency and 12W output power", Microwave Symposium Digest, 2008 IEEE MTT-S International, pages 1147-1150.
7. Q. Hao, J. Benedikt, and P. J. Tasker, "Nonlinear Data utilization: From Direct Data Lookup to Behavioural Modelling", IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 6, June 2009
8. D. M. FitzPatrick, J. Lees, A. Sheikh, J. Benedikt, and P. J. Tasker, "Systematic Investigation of the Impact of Harmonic Termination in the Efficiency Performance of Above Octave Bandwidth Microwave Amplifiers", 39th European Microwave Conference, 2009.