A COMPARISON OF TWO DELAY LINE DISCRIMINATOR IMPLEMENTATIONS FOR LOW COST PHASE NOISE MEASUREMENT

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Abstract

This paper focuses on low cost production testing of the far-out phase noise of PLL ICs using the delay line discriminator method. It describes two different delay line discriminator (DLD) implementations for phase noise measurements at large frequency offsets from the carrier. The calibration method using an FM calibration signal is described in detail, both mathematically and graphically. The results show good comparison with laboratory based phase noise measurement equipment.

1. Introduction and Background

In the past PLL solutions for RF wireless applications consisted of separate components consisting of a voltage-controlled oscillator (VCO), frequency synthesizer and loop filter. The VCO was usually sourced from a company who specialized in VCOs or the VCO design might have been done by the RF wireless equipment designer. The VCO would have been costly and the vendor would have to production test the key specifications. One of the most critical specifications of these VCOs would have been its phase noise performance. Phase noise is a measure of the amount of random frequency fluctuations of an RF signal. Phase Noise performance of a VCO would have been tested thoroughly during laboratory evaluation. Phase Noise measurement systems in the past were complex, bulky and not very production friendly. Vendors would have had to include the bulky equipment in their production facility to test the phase noise specifications. Test times were slow and the phase noise equipment was very expensive. One early system was the HP 11729 phase noise measurement system.

Today with the advances in semiconductor process technology, the VCO is frequently integrated with the RF frequency synthesizer thus providing the end customer with a more integrated solution. In some cases the loop filter is integrated on the chip giving the user a complete PLL block that needs only some SPI commands to setup the RF output frequency. Many tests have to be performed on these chips to guarantee the quality of the solution. These tests need be executed in the minimal time in order to keep the test cost to a minimum. Receiver blocking specifications and transmitter spectral masks limits will demand low phase noise performance from these VCOs. Adding an expensive phase noise test system such as those available from Agilent and Rohde and Schwarz is an easy way to testing the VCO phase noise performance of these PLL chips. Adding a small number of these systems to the production facility may not be the most economic option. Current ATE for chip solutions allow phase noise to be measured but

not to the high performance of the bench type phase noise measurement systems. If one could add a low cost solution that integrates easily with the existing ATE, this would be extremely useful for guaranteeing the phase noise specifications of PLL solutions.

Low cost phase noise measurements have been implemented by some engineers in the past. W. Suter described a low cost solution for under $250 in 1995 [1]. His solution tested the VCO phase noise using the delay line (frequency) discriminator (DLD) method [2]. His results were reasonable and good enough for the VCO under test. Teradyne engineers in 2002 described a phase noise solution that was integrated into the ATE [3]. The solution was based on down-converting the RF signal to a low frequency intermediate frequency (IF), implementing a delay line (frequency) discriminator (DLD) at the IF frequency and then calculating the resultant phase noise. However, this solution is not adequate enough to measure the far-out phase noise of current PLL solutions as the LO used in the down-conversion process can dominate the noise measurement. Ferrario et al. at IBM published a low cost circuit for measuring VCO phase noise at 3MHz offset [4]. Details on RF frequencies and results were not available. There have also been cases where engineers have built their own phase noise measurement circuits in the lab for evaluating phase noise of a small number of units. P. Goyal described a lab based delay line discriminator for measuring phase noise offsets at far-out frequencies where his lab equipment did not have sufficient phase noise floor [5]. M. Smith described fully an implementation of the phase detector method for measuring the phase noise performance close to carrier [6].

This paper compares two DLD implementations for measuring good far out phase noise performance of RF PLLs. Section 2 gives a short summary of phase noise measurement methods and mentions the basics of the delay line frequency discriminator (DLD). Section 3 describes the two different delay line frequency discriminator implementations that could allow production testing of the far-out phase noise performance of RF PLLs. Section 4 describes the laboratory measurement and calibration of both DLD implementations.

2. Phase Noise Measurement

Phase noise is a measure of the random frequency fluctuations of an RF carrier. It is usually specified in dBc/Hz. For example -90dBc/Hz at 10kHz offset, means that at 10kHz offset from the carrier, the noise in a 1Hz bandwidth is 90dB below the carrier.
One of the easiest methods to measure the phase noise of an RF signal is to down-convert the RF signal to a low frequency IF and then measure the spectrum of the IF. It is the method used in traditional spectrum analyzers and is also currently used in ATE for measuring the phase noise of a signal. The measurement receiver should have a lower noise floor than the signal to be measured and any local oscillator in the receiver must have much better phase noise than that of the signal to be measured [7]. This method is usually good enough for measuring phase close to carrier at levels above -100dBc/Hz . The noise over a finite bandwidth can be summed and compared to the carrier power giving an integrated noise ratio in degrees rms. This measurement parameter is a good test check of the phase of the frequency synthesizer components that include the prescaler, low noise charge pump, phase frequency detector and the VCO. For frequencies less than the PLL loop bandwidth, the phase noise performance is dominated by the charge pump, PFD, reference and RF dividers. Outside the loop bandwidth the

phase noise tends to be dominated by the VCO phase noise. At large offsets from the carrier, the VCO phase noise can be too close to the phase noise of the local oscillator (LO) of the measurement receiver [8].

Measuring the VCO phase noise is usually done on dedicated bench equipment from Agilent Technologies, Rohde & Schwarz or other vendors who specialize in phase noise measurement systems. Systems that measure low phase noise performance of VCOs at higher frequency offsets use a method of demodulating the RF carrier and amplifying the low noise signal at the demodulator output. The two most popular methods are the (i) delay line (frequency) discriminator (DLD) method and the (ii) phase detector method [9]. The theory of operation and worked examples of the methods are explained thoroughly in application notes for the HP11729C phase noise measurement system [2] [10]. The phase detector method phase locks the DUT to a very low phase noise reference source using a narrow bandwidth PLL based on a mixer type phase detector and the resultant signal at the mixer output is proportional to the phase noise of the DUT. The PLL has a narrow capture range and the system can suffer from injection locking problems. The main focus of this work is concerned with the DLD as it is easier to implement and debug for far out phase noise frequency measurement.

2.1 Delay Line Frequency Discriminator Basics

In the delay line (frequency|) discriminator (DLD) method, the RF input signal is first split into two paths [2], see fig.1. One path is applied to the LO port of a passive double-balanced mixer mixer acting as a phase detector. The other path is passed through a delay line and then through a phase shifter. The delay line converts frequency fluctuations of the RF into phase fluctuations relative to the signal at the LO input to the phase detector. The phase shifter is used to achieve quadrature between the RF and LO port of the phase detector. The phase detector then converts the phase fluctuations into their voltage equivalent which is low-pass filtered, amplified and digitized. This signal is proportional to the phase noise of the input RF signal.

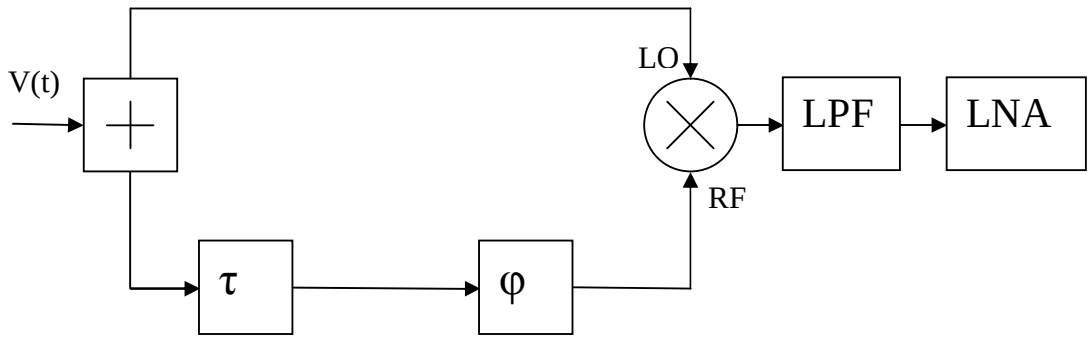

Fig. 1 Delay Line Frequency Discriminator

The DUT phase noise is described as a narrowband FM signal [2]

$$V(t) = Vs.\cos(2\pi f_o t + \frac{\Delta f}{f_m}\cos 2\pi f_m t) \qquad (1)$$

with a modulation index, $\frac{\Delta f}{f_m}$ or sometimes described as β, which is the peak phase deviation of the modulating signal. For the FM representation, peak frequency deviation term is Δf , and f_m is the rate . The magnitude of the phase noise is β and the frequency offset at which the phase noise is being observed is f_m .

Appendix A in [2] derives the transfer response of the delay line discriminator. Using some trigonometric identities and the signal description in (1), and assuming that there is 90 degree quadrature between the mixer inputs, it is shown that the filtered signal at the output of the phase mixer acting as a phase detector is

$$\Delta V = K_\varphi . 2\pi\tau_d . \Delta f . \frac{\sin(\pi f_m \tau_d)}{\pi f_m \tau_d} \qquad (2)$$

This output voltage is proportional to the peak deviation of the FM modulation, the delay line delay in seconds and the K_φ of the mixer. The output also has a sinc response in it, exhibiting a null in the frequency response at $f_{null} = 1/\tau_d$. This null in the frequency response is a good checker than the DLD circuits are functioning correctly. Assuming that the measurement frequency offset is less than $f_{null}/2\pi$, then the voltage output of the discriminator can be truncated to

$$\Delta V = K_\varphi . 2\pi\tau d . \Delta f \qquad (3)$$

$$\Delta V \cong K_d \Delta f , K_d = K_\varphi . 2\pi\tau_d [V / Hz] \qquad (4)$$

So the voltage output of the discriminator is proportional to the peak frequency deviation of the RF input signal. K_d is usually referred to as the discriminator constant. If K_d is known, then the amount of peak frequency deviation at the modulation frequency offset (or FM rate) can be measured. This allows us to calculate the modulation index, β, which we assume is the double sideband phase noise amplitude. It is this assumption that forms the basis for DLD phase noise measurement. The AM noise on the signal is assumed to be well below the phase noise. If DLD output signal can be averaged and processed in the background DSP of the ATE, then this method could offer a lower cost advantage over adding expensive phase noise analyzer systems to the ATE

3. DLD Component Selection

Two implementations of the DLD were carried out. The first was used on an internal RF ATE used by ADI. The main restriction on this was the mechanical headroom on the tester side of the PCB. This was only 1 inch in places and did not allow the use of connector based components. Thus all components were surface mounted. The second DLD was implemented using connector based components. The intention is that these components will be inserted in a more modern tester that has sufficient headroom to allow the DLD to be attached to the tester side of the PCB. It also makes is easier to debug and improve the performance in the laboratory.

3.1 Implementation of Surface Mount DLD, *DLD1*

The splitter was a SCN-2-22, Mini-Circuits type. The phase detector used was a MACOM SMG4 Passive DBM, a double balanced mixer which requires +7dBm at it's LO port. The delay line was a 2.1-2.17GHz delay filter, TMD-2140 from K&L Microwave, with a typical delay of 10ns. It has a typical insertion loss of 3.5dB. The phase shifter used for achieving quadrature between the two mixer ports is a narrowband type, SV Micro VP212N. Phase adjustment is provided by varying the voltage on VPHS pin. 200 degrees of phase can be easily achieved from 0 to 4V. The total cost of these components was less than $350. A photo of this DLD is shown in fig.2. The circuit was placed on the tester side of the PCB on a Rogers's 4350 substrate. SMP connectors were placed at the main input, the VPHS input of the phase shifter and the IF output of the SMG4 mixer. This allows the circuit to be evaluated on the bench using lab-based equipment. Due to the narrowband nature of the phase shifter and the delay filter, this circuit only operates in the 2.1-2.2GHz band.

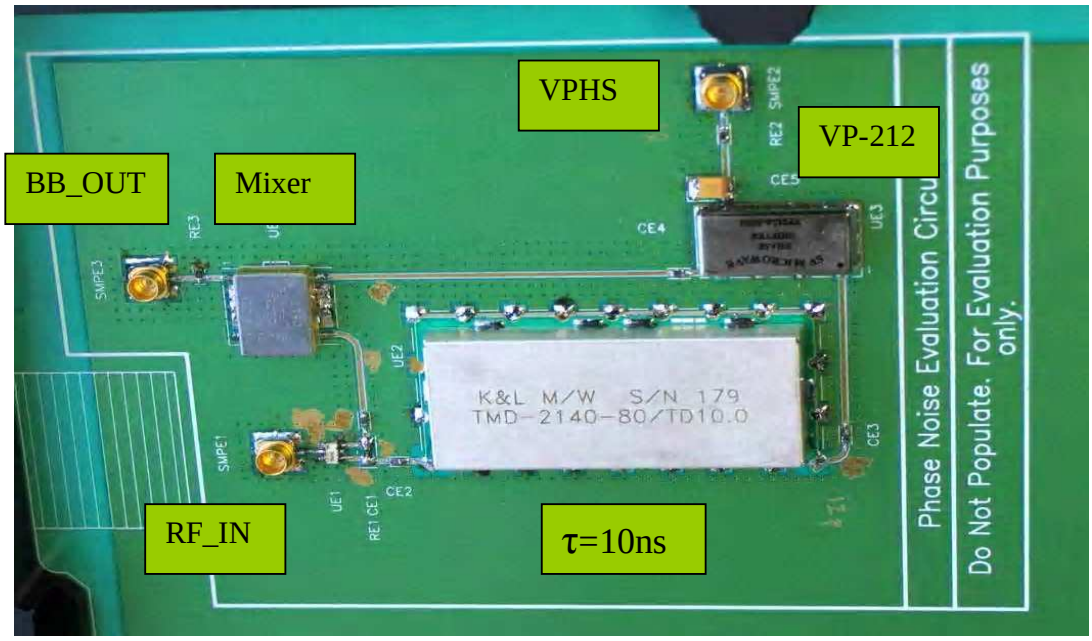

Fig. 2 Surface mount DLD, DLD1

3.2 Implementation of Connector Based DLD, *DLD2*

The second DLD is made up of connector based components The splitter used for this experiment was the ZN2PD2-50 from Mini-Circuits, a wideband splitter operating to 5GHz. It has a typical insertion loss of 3.8dB. The phase detector was the MY85C from MACOM . It is a double balanced mixer that can be used as a phase detector. It operates at a minimum LO frequency of 2GHz and needs +7dBm to drive the LO port. The phase shifter is a mechanical type, Model 980-3 from Aeroflex Weinschel. Phase trimming is performed by adjusting a screw and there is a self-locking mechanism. It is very low insertion loss and 85degrees of phase shift can be achieved at 3GHz. The delay line was a custom design by Rosenberger Micrcoax. The intention was that the delay line would be attached to external SMA connectors on the side of the test head, a feature that is

available on the Teradyne Microflex RF tester. The connectors then connect via short cables to OSP connectors for mating to the test board, It has a typical delay of 30ns, insertion loss of 4.5dB at 3GHz, and is assembled as a 600mm coil of UT141 cable weighing less than 300grams. A photo of this DLD is shown in the fig. 3.

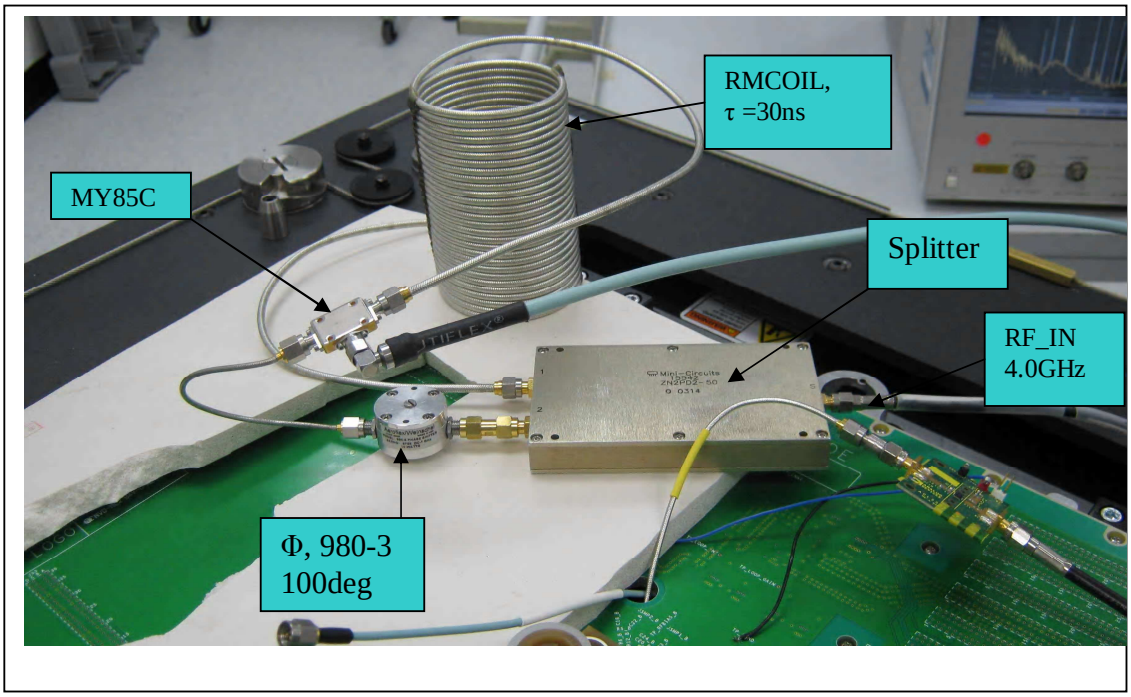

Figure 3. DUT Test Setup, DLD2

4. Calibration & Measurement

4.1 Calibration

One method for measuring the Kd is to measure each of the insertion losses of the components between the RF input and the mixer plus also measuring the K_φ of the mixer by applying two slightly different frequencies and measuring the amplitude of the output beat frequency. This is OK for a lab based measurement and it also has the weakness that each of the components must be disconnected from the measurement as mentioned in [5]. For the DLD method to be robust for production, it is better to use the FM calibration method as described in [2]. There will be slight differences in the RF insertion losses from one DLD to the next. Another issue is that each DUT will not have the same RF output power. There will be a spread over a few dB and there could also be lot to lot variation on the RF output power parameter. The RF power at the input to the DLD also has an impact on the Kd of the overall system. For these reasons, every DUT will have to have the FM calibration performed on it. This must be quick and it is possible that the calibration and the measurement could be performed in the same capture. A known amount of low modulation index ($\beta < 0.1$) FM is enabled on the DUT. The baseband signal is digitized and the tone at the FM offset frequency is measured in dBV. From this measured tone level and the known modulation index the K_d of the DLD setup at the DUT power can be calculated.

4.2 Maintaining quadrature.

For measuring one unit in the lab, quadrature between the two inputs to the mixer can be set by adjusting the voltage on the input to the VPHS of the VP212 phase shifter. For measuring many units in production, this phase shifter would be adjusted on a DUT by DUT basis. This will minimize the DC level at the mixer output and reduce errors in the phase noise measurement and calibration. The disadvantages with using this circuit are that the phase shifter only operates over a small bandwidth so a new carrier frequency measurement will need a new phase shifter. It also has higher insertion loss than the mechanical type which will reduce the overall K_d of the system. The mechanical type phase shifter will only be adjusted once at the very first lot setup. A locking mechanism will ensure that the phase shift will not vary. Monitoring the quadrature for every measurement will be implemented in the baseband section to ensure that the phase shift between the mixer inputs is either zero or else at least within acceptable limits. It is mentioned in appendix E of [2] that a 10deg deviation from quadrature (proportional to the cosine (quadrature deviation) will result in ±0.35dB error in the overall phase noise measurement.

4.3 Lab based measurement of both DLDs

Before a DLD circuit can be considered for a production implementation, it is worth setting up the measurements in the lab with bench equipment. A signal source that has low modulation index FM (ESG400) is used for the calibration and the measurement of the *DLD2*, the connectorized type. In this case the measurement instrument used is the E5052B signal source analyzer from Agilent technologies. The source phase noise is measured using the phase noise measurement option and the DLD baseband noise measurements can be compared with this. Figure 4 shows the spectrum analyzer plot of a 4GHz signal, +9.78dBm output with 1kHz deviation and 50kHz rate FM, β=0.02 . The level of the FM spur is 40.35dB down on the carrier close to the theoretical. This 4GHz signal initially with the FM off is applied to the splitter input and the phase shifter is adjusted until there is 0V DC at the mixer output. The FM signal is then enabled and the low pass filter output is connected to the BBNOISE input of the E5052B. Fig. 5 shows the frequency spectrum on a 40MHz span. The output voltage noise increases linearly at greater than 1MHz and then at further offsets the sinc function kicks in. Note the null in the plot at 34MHz which corresponds to a total delay in the path of 29.4ns.There is a distinctive tone at 50kHz offset and the level of this tone, P_{cal}, is proportional to the peak deviation of the input FM signal and the DLD constant, K_d. Using the notation in the appendix C of [2], the K_d can be calculated in dB as

$$K_d = P_{cal} - (\Delta_{cal} + 20\log f_m + 3dB) \tag{5}$$

In this example,

$$K_d = -94.8dBV - (-40.35 + 20\log 50k + 3dB) = -151.429dBV/Hz$$

On the same plot, if we note the output voltage at 4MHz offset frequency, -159.77dBV the single sideband phase noise can be calculated from

$$L(f) = Pnoise - K_d - 20\log f_m - 3dB \tag{6}$$

$$L(f) = -159.77dBV/Hz + 151.429/Hz - 20\log(4e6) - 3 = -143.38dBc/Hz$$

The source was measured before and after using the phase option of the E5052B and the phase noise at 4MHz offset was -143dBc/Hz. The plot is shown in fig. 6. It can be seen that the phase noise is fairly flat at greater than 2MHz and for this flat response, the DLD baseband noise output is increasing linearly with frequency offset as expected. The valid region for doing the phase noise measurement of this source is from about 2 to 5MHz without without sinc() correction. The PCB DLD, *DLD1*, was setup and measured at 2.1GHz with a 12dbm input using the same method above and we were able to measure -148dBc/Hz at 10MHz offset frequency. The generator measured -149dBc/Hz on the phase noise measurement option. The null frequency in this case was at 84MHz and 10MHz was well within the linear behaviour of the output response. One mistake that made during early debug work was not measuring the cal tone output at baseband correctly. When measuring this tone, be sure that the spurious measurement is setup to measure the spur not normalized to a 1Hz bandwidth.

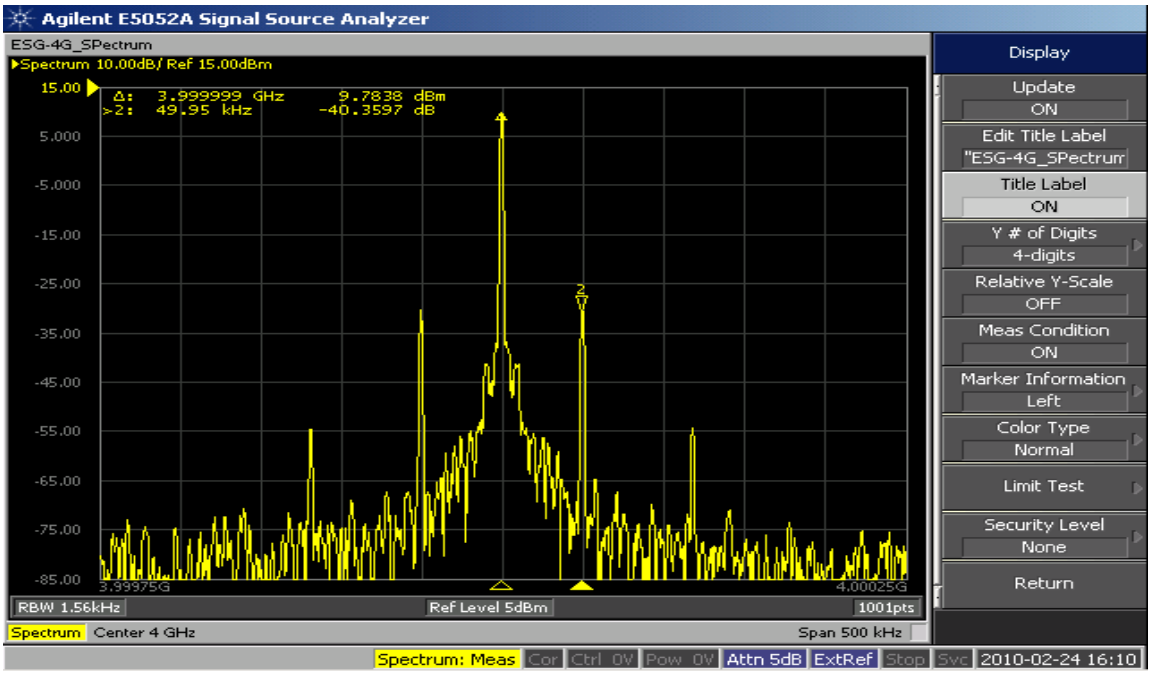

Fig. 4 FM spurs on DLD2, 4.0GHz , 10dBm

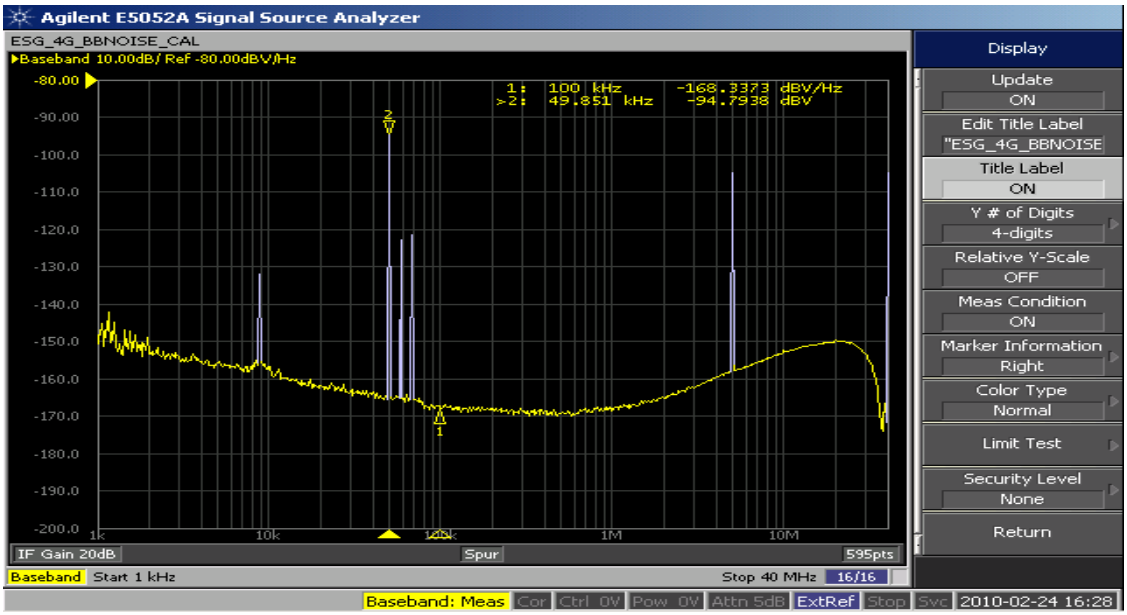

Fig. 5 BNNOISE with FM cal tone at 50kHz, DLD2

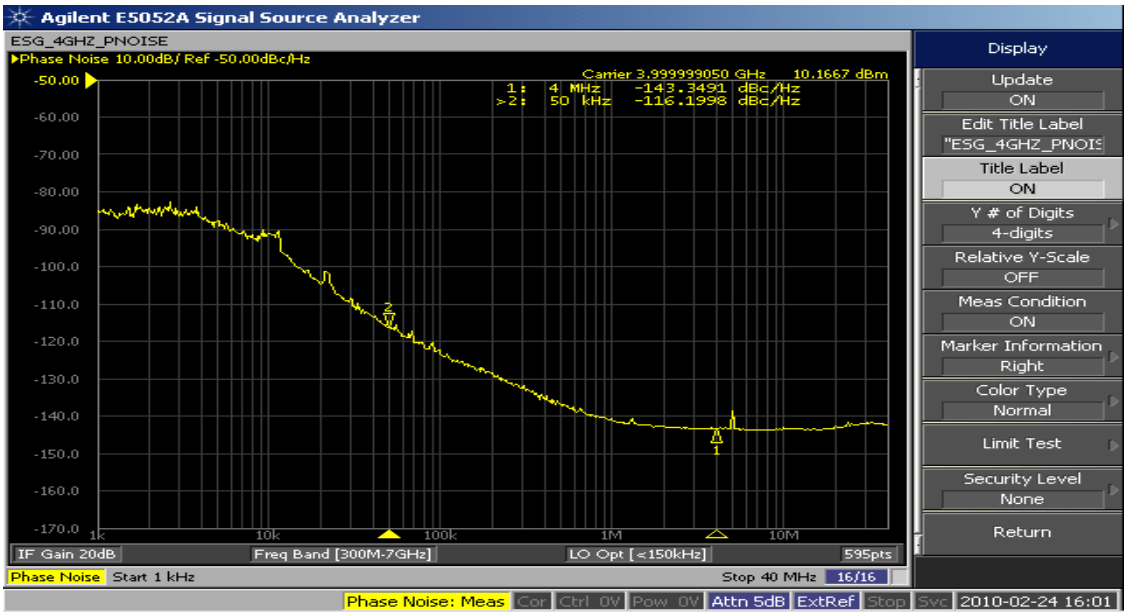

Figure 6. E5052B Phase Noise Plot

The measurement noise floor of the setup is measured by removing the delay line, replacing it with a short cable and adjusting the phase shifter for 90deg quadrature. A plot showing the baseband noise output and the measurement noise floor for a 4GHz DLD2 setup is shown in fig.7. At 4MHz offset, the baseband noise signal is 12dB greater than the measurement noise floor.

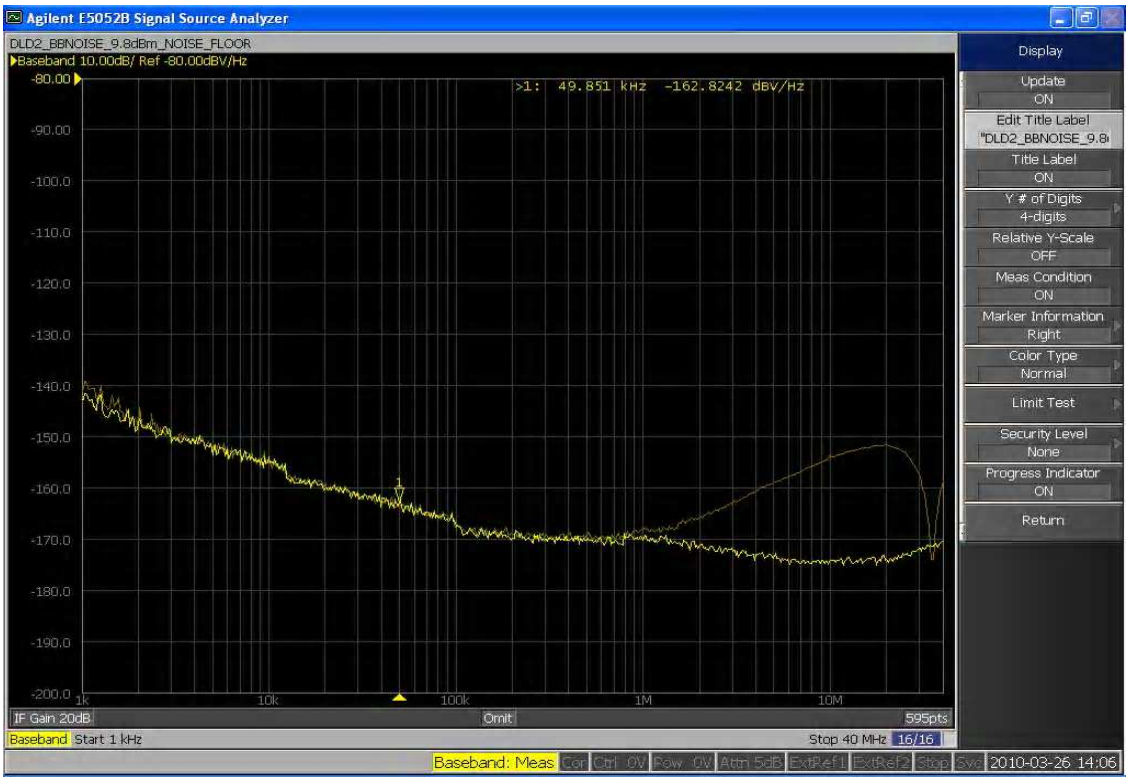

Figure 7. DLD2 BBNOISE and Noise Floor (delay line replaced with 6. in cable) , 4GHz setup

Table 1 summarizes the features and bench results of both DLD implementations.

DLD TYPE	DLD1	*DLD2*
Implementation	PCB (SMP) surface mount	SMA / Components
Delay , τ	~10ns	~30ns
Phase Shift	Elect., 200deg @2.1GHz	Mech., 85deg @ 3.5GHz
Cost	< $400	<$500
Frequency	2.1GHz, +12dBm	4GHz, +9.8dBm
$L(f)$, DLD Method	-148.5dBc/Hz @ 10MHz	-143.38dBc/Hz @ 4MHz
L(f), E5052B	-149.1dBc/Hz @ 10MHz	-143.34dBc/Hz @ 4MHz

Table 1 DLD1, DLD2 comparisons

6. Conclusions

In this paper, I have presented implementations of the delay line frequency discriminator for low cost phase noise measurement of RF PLL ICs far-out phase noise. These results are comparable with laboratory based equipment over a small frequency offset range. The DLD will only have a narrow span of measurement range depending on the DUT phase noise and delay line characteristics. DLD2 is a better candidate for integration in a production test environment due to its wider bandwidth compared to the

narrowband DLD1. Low phase noise measurement using the DLD is difficult as the voltages levels are in the range of less than -150dBV.

Finding higher level DSB mixers that can be used as phase detectors in combination with higher RF input signal levels could be investigated for further improving the phase noise measurement dynamic range. The next step in this work is to take the DLD2 implementation and integrate it as part of an RFIC ATE solution. This will require adding circuits for monitoring the quadrature, filtering the high frequency components and amplifying the low noise signal before it is captured on the ATE digitizer. Finding a suitable means of applying an FM signal onto the locked DUT will have to be investigated also.

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