A HIGH LINEARITY FMCW SWEEP GENERATOR

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Linearly swept Frequency Modulated Continuous Wave (FMCW) sources are widely used as the basis for RADAR systems. This approach enables good resolution and range without the need for short pulse, high peak power transmitters and is thus well suited to solid state systems and millimetre wave operation. Cobham Technical Services have developed a K-band sweep generator with the linearity and wide sweep range necessary to form the heart of a high resolution RADAR system. The sweep generator is fully synthesised using a hybrid architecture with both DDS (Direct Digital Synthesiser) and PLL (Phase Locked Loop) elements. This compact solution generates sweep rates of 1kHz, with a deviation of 1.5 GHz or 8%. The spurious levels are typically less than -80dBc and the sweep linearity better than 0.01%. The frequency source has been multiplied up to V-band (75 GHz) where it enables an instrumentation RADAR to achieve better than 3cm resolution.

FMCW Radar Principles

An FMCW RADAR continuously transmits a swept frequency carrier. The propagation delay to the target and back causes a frequency difference between the transmitted signal and the received signal.

Mixing a sample of the TX signal with the RX signal results in an IF waveform containing frequency difference components. With a linear sweep the frequency difference between the TX and RX signals is proportional to the target range. Digital FFT analysis can be used to partition the IF signal into a number of frequency or range bins. Figure 1 shows the basic hardware configuration, while Figure 2 illustrates a sweep waveform.

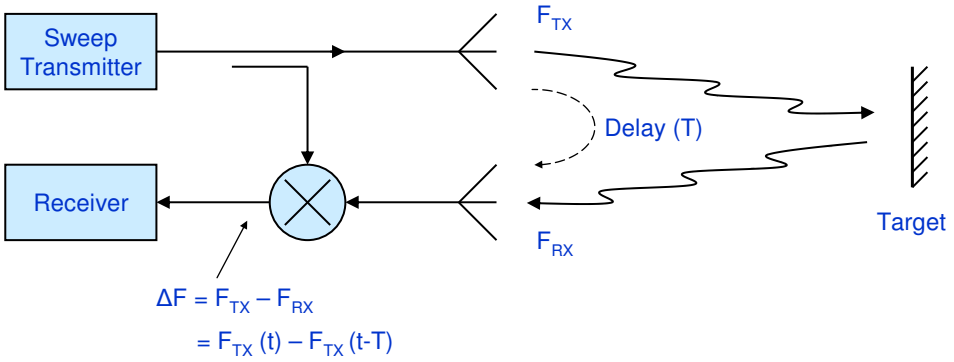


Figure 1 FMCW RADAR Architecture

Various sweep patterns are possible. In this instance a symmetrical triangular sweep has been employed. This has two features that are of particular interest:

Doppler Discrimination: The symmetrical up and down sweep enables the Doppler frequency of a moving target to be separated from the range related terms by using approriate IF processing.

Ease of Realisation: The triangular waveform avoids the sharp transitions inherent with other popular waveforms, such as the sawtooth, which are difficult to achieve in a well controlled manner.

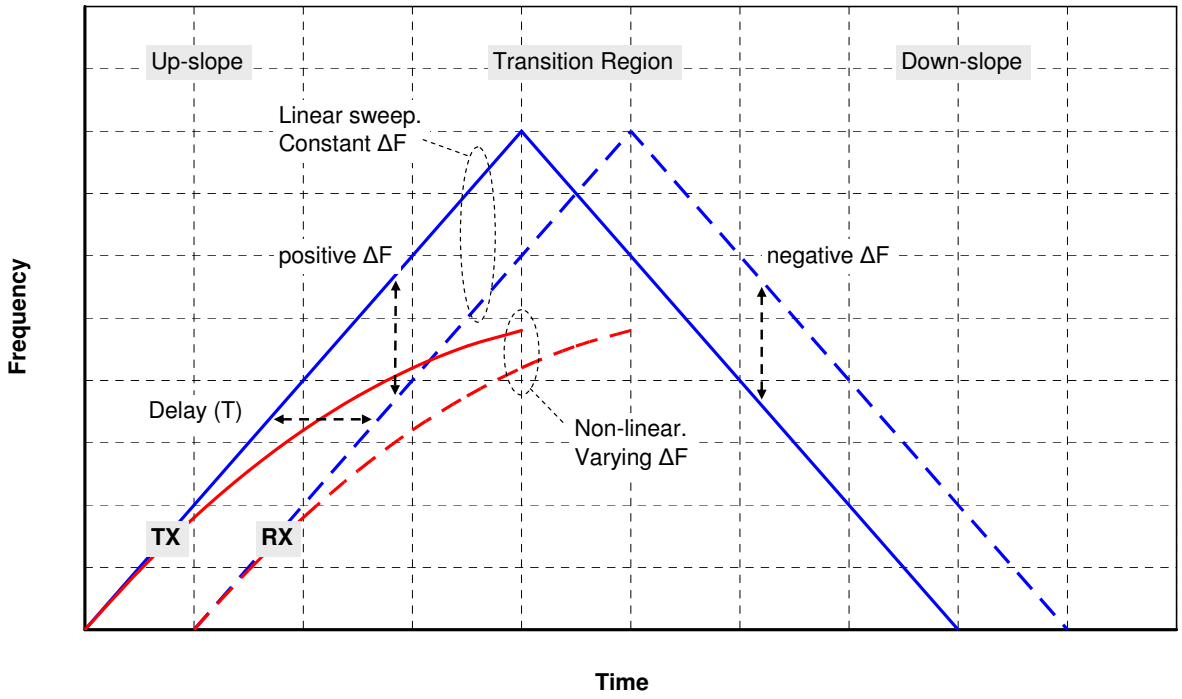


Figure 2 Triangular Sweep

Key Equations

The frequency difference as a function of range $\Delta F(R)$ is:

$$\Delta F(R) = \frac{2.R.S}{c}$$

where R is the target range and S is the frequency slope (Hz/s)

The achievable range resolution (ΔR) is defined as follows:

$$\Delta R = \frac{c}{2.BW}$$

where c is the speed of light and BW is the sweep bandwidth

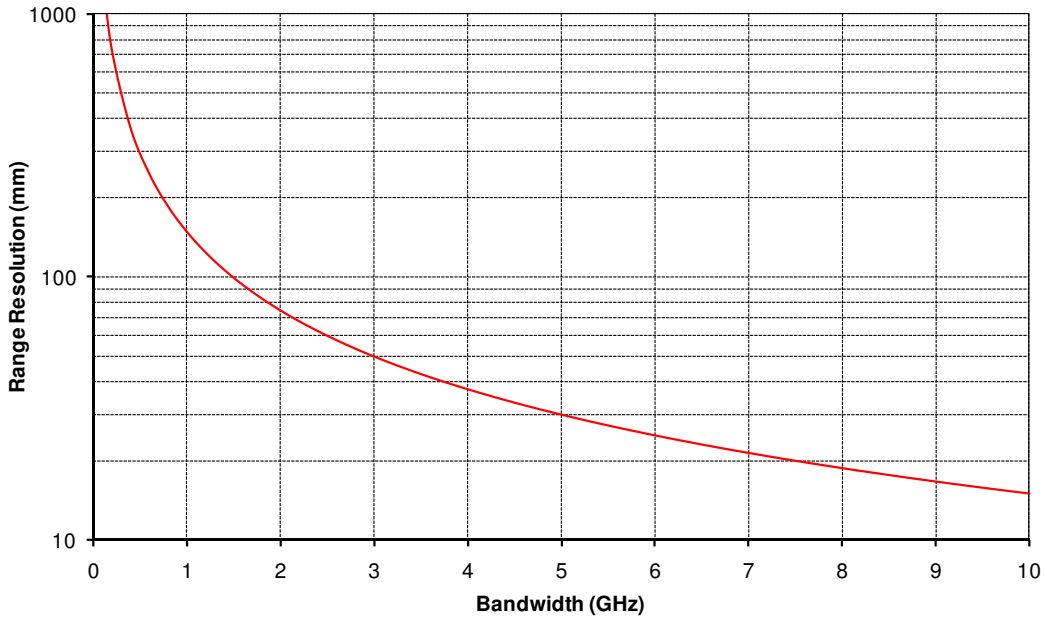


Figure 3 Resolution versus Bandwidth

Typical Sweeper Implementations

Open Loop VCO

A Voltage Controlled Oscillator (VCO) is controlled by a linear ramp voltage or a ramp that has some form of polynomial correction added to counteract the inherent non-linearity of the VCO transfer function. The correction can also be performed digitally by using a Look Up Table (LUT) and DAC to store pre-calibrated control data. This approach is capable of modest linearity and high sweep speeds. The main drawback is that the required calibration/correction is not static over time and temperature and thus limits the achievable linearity.

VCO and Frequency Discriminator

The basic ramp driven VCO is supplemented with a frequency discriminator that generates a voltage output proportional to frequency. This provides a feedback signal that can be used to implement closed loop correction and overcome the VCO non-linearity. Unfortunately the analogue frequency discriminator has limited performance and cannot achieve the accuracy required for high resolution, wide-band systems.

Synthesiser Subsystems

The following sections give a very brief introduction to DDS and PLL synthesiser architectures. These are key parts of the hybrid synthesiser described later.

PLL (Phase Locked Loop) Synthesiser

The PLL uses a negative feedback loop to force the phase derived from the output of the system (The VCO) to match the reference frequency phase. The inclusion of a frequency divider (÷ N) in the feedback path forces the output to be multiplied (x N) such that the reference phase and the output of the divider are locked together.

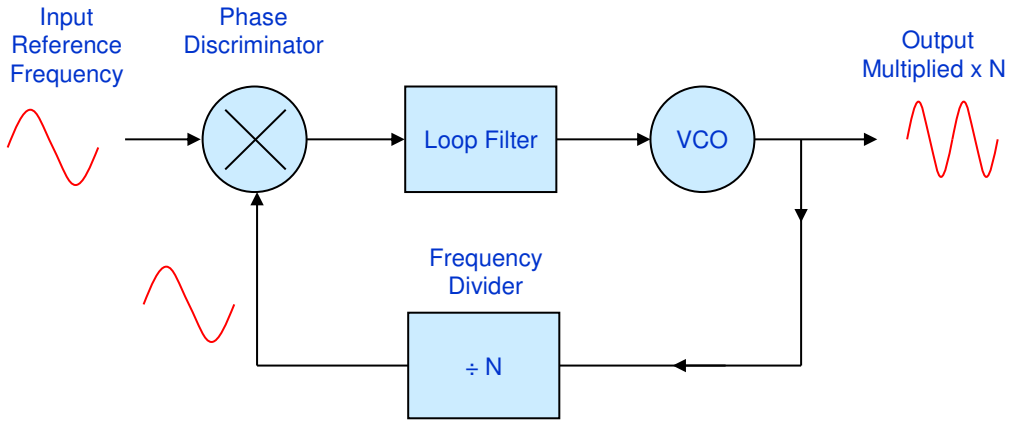


Figure 4 PLL Synthesiser

Modern PLL designs are extremely flexible with programmable frequency dividers in the feedback path and the reference input path. In principle these devices can be re-programmed 'on the fly' to generate frequency sweeps. In practice, constraints pertaining to programming speed, achievable divider ratios, phase comparison frequency, and loop bandwidth make it difficult to generate fast, clean, linear ramps.

DDS (Direct Digital Synthesiser)

The output of the DDS is created by reconstructing a sinewave using a look up table and a DAC. The table contains amplitude values as a function of a phase index. Stepping through the table generates a sinewave. Only phases up to 2π are required; beyond that the table wraps back around and starts over again using modulo 2π indexing. The frequency of the resulting output is controlled by fixing the step rate and changing the phase increment in proportion to the frequency required. This is easily implemented using a programmable logic system; essentially an adder (or accumulator) to store and increment the phase based on the 'frequency word' setting.

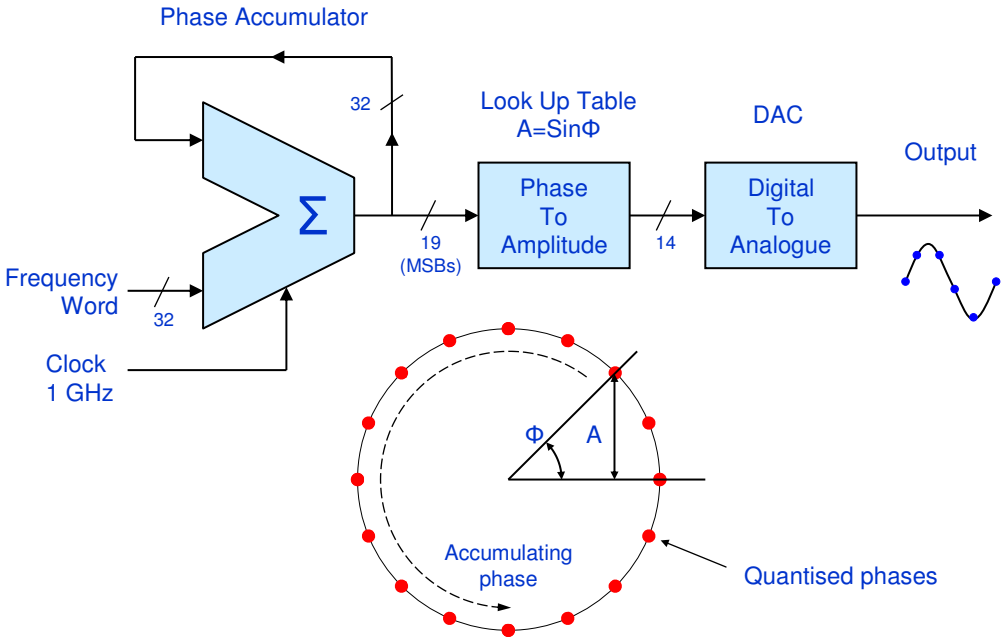
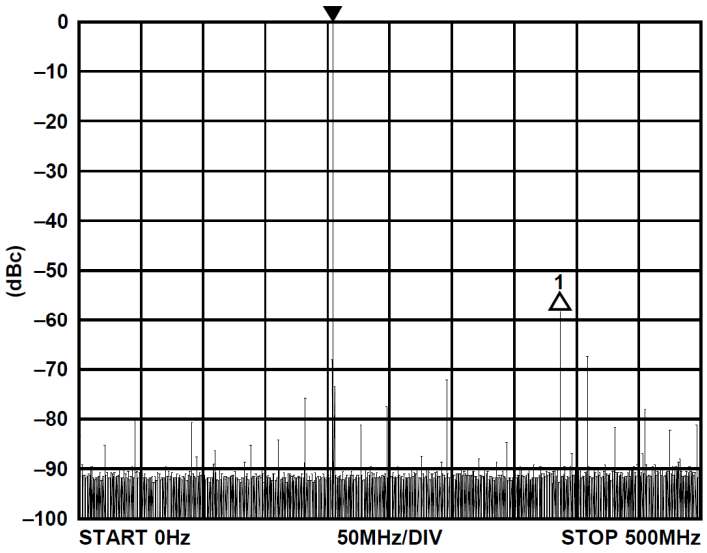


Figure 5 DDS Synthesiser Core

The Analog Devices AD9910 is a flexible, high speed, single chip DDS solution. It is capable of generating frequencies from 0 Hz up to approximately 400 MHz using the maximum 1 GHz clock. The frequency is inherently very accurate due to the high resolution 32 bit processing. Because it is a sampled and quantised system the output spectrum contains significant spurious products, typically at levels around -55 dBc.



Wideband SFDR at 204 MHz, REFCLK = 1 GHz

Figure 6 Typical DDS Spectrum (from Analog Devices AD9910 data sheet)

An extension to the basic DDS core enables generation of extremely accurate frequency ramps. By using some additional logic the frequency word controlling the instantaneous frequency of the DDS core can be varied linearly with a ramp. The logic sets the start and stop frequencies and manages the switch between ramping up or down.

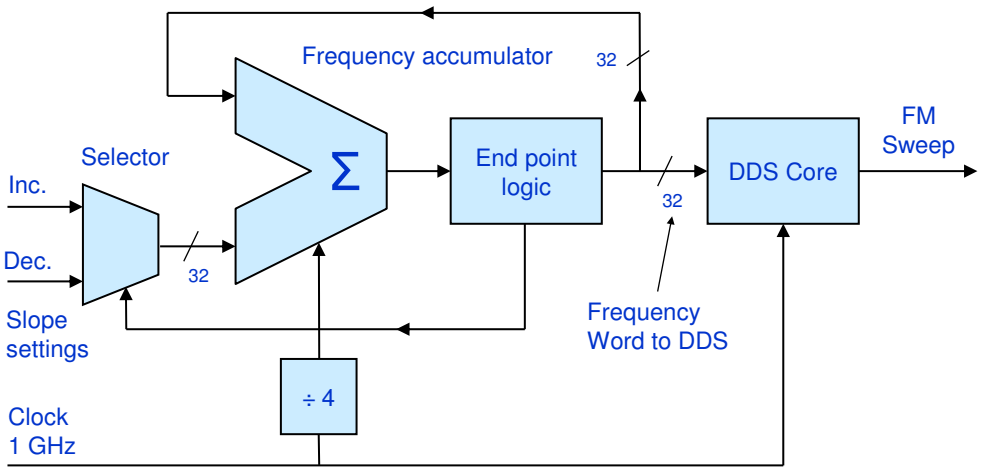


Figure 7 DDS With Frequency Ramp

In the case of The Analog Devices AD9910, the DDS internally updates the frequency every 4 clock cycles, or 4ns. This equates to 250,000 discrete steps within a 1 ms frequency sweep.

Hybrid Synthesiser

Two key features of the architecture are:

Minimum DDS multiplication factor by use of frequency translation and,
Integrated tracking filter function to smooth steps and reduce DDS spurious levels.

Minimising DDS Frequency Multiplication

Frequency multiplication increases the level of spurious signals by an amount equal to 20log(n) where n is the multiplication factor. Thus one of the key design aims for the hybrid synthesiser is to use the lowest practical DDS frequency multiplication factor (in this case x8). This means dissociating sweep bandwidth and centre frequency so that both aspects can be dealt with independently. In the architecture of Figure 8 the DDS provides the reference input to a modified PLL system. The feedback path of the PLL includes a divider to achieve the required closed loop bandwidth multiplication. To achieve the desired output frequency (18.75 GHz) the feedback path of the PLL also includes a fixed frequency downconverter. The downconverter within the feedback path effectively adds an offset frequency to the final VCO output.

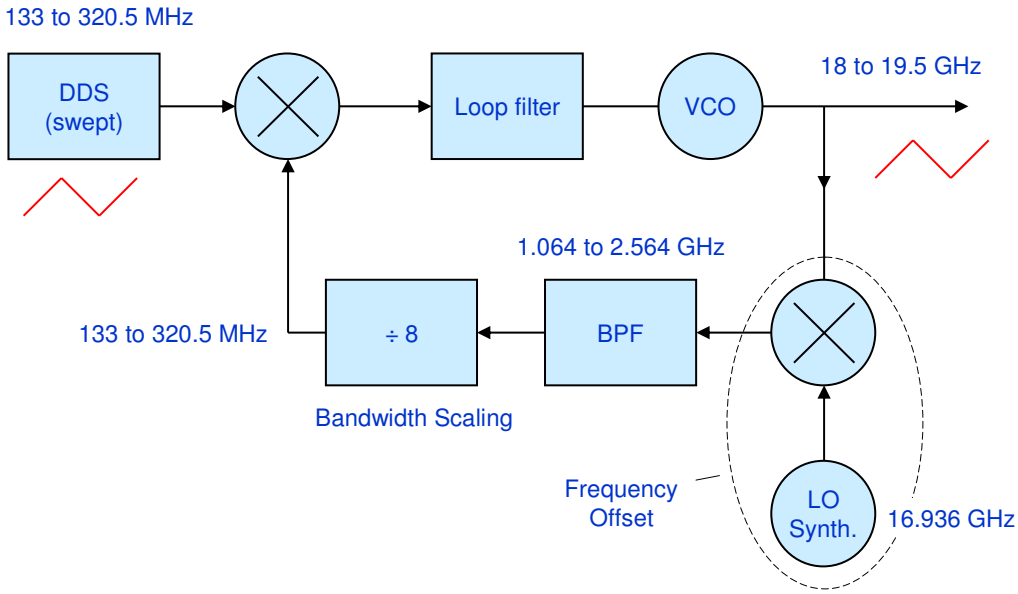


Figure 8 Hybrid Synthesiser

Tracking filter

In an ideal situation the output from the VCO does not contain any non-harmonic spurii. However, in practice, unwanted signals reach the VCO control port and the resulting modulation causes spurious sidebands at the VCO RF output. The low pass loop filter is designed to minimise the bandwidth of the spurious modulation while maintaining adequate loop dynamics. From the DDS's perspective the PLL appear as a tracking filter. The PLL tracks the reference input frequency and the low pass loop filter limits the bandwidth of the VCO control signal such that the unwanted sidebands are constrained to a narrow, symmetrical bandwidth around the carrier. The combination of fast DDS frequency update (4ns) and relatively low PLL loop bandwidth (200 kHz) effectively eliminates any granularity in the output. At carrier offsets less than the loop bandwidth the DDS spurious levels are increased by 18dB (to typically -37 dBc) due to the multiplication factor (x8). For offsets greater than the loop bandwidth the DDS spurii are progressively attenuated. Appropriate choice of loop filter bandwidth, in this case around 200kHz, means that most of the spurious components in the output of the DDS (up to 400MHz) are attenuated and the end result is an extremely clean wideband spectrum.

Spurious levels better than -80dBc are easily achieved over broad bandwidths. The broadband noise floor of Figure 9 is the spectrum analyser measurement limit, with no synthesiser spurious components visible.

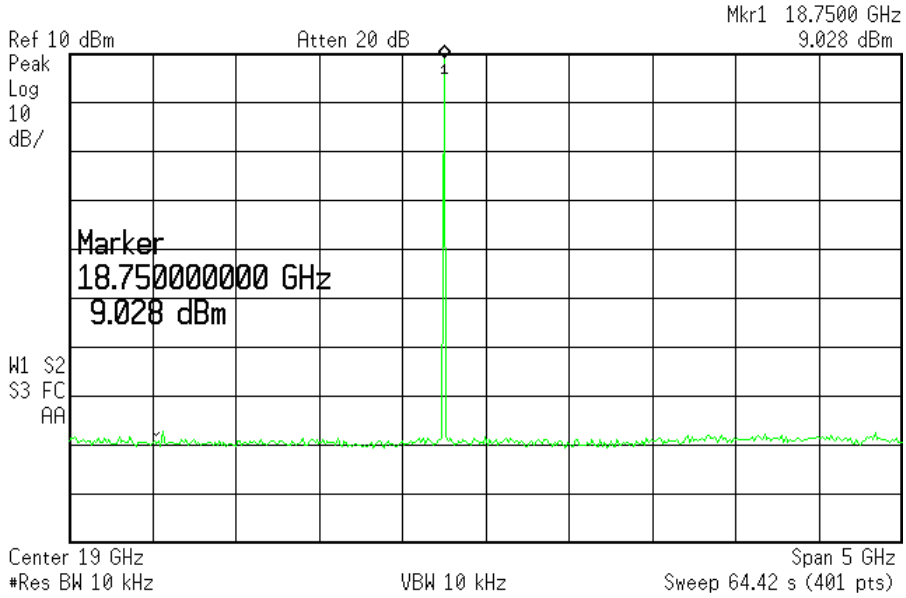


Figure 9 Wideband Spectrum

The major DDS spurious frequency components are not fixed but are related to DDS output frequency. In this case, with a swept frequency output, unfiltered spurious components within 200kHz of the carrier exist for just a very small part of the sweep and thus are of minimal significance when their overall contribution is considered. Figure 10 shows the close to carrier spectrum dominated by phase noise with two small discrete spurious signals at +/- 1.5MHz offset.

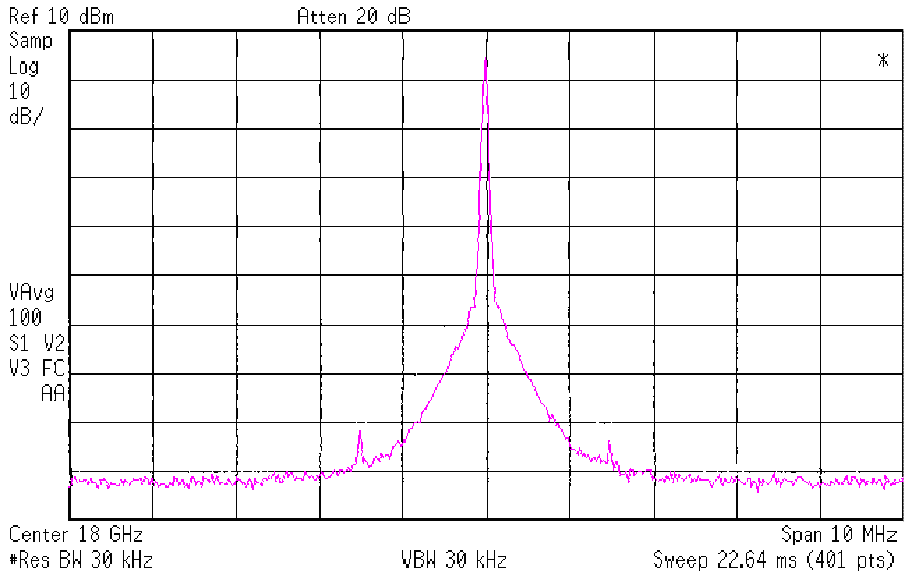


Figure 10 Phase Noise

Figure 11 shows the VCO control voltage in purple and the loop error (phase discriminator output) in red. The control voltage is essentially triangular, reflecting the up/down sweep pattern, but sharp eyes might just notice that the sides are not straight because of the non-linearity of the VCO transfer function. The error voltage confirms that the loop is phase locked throughout the whole cycle and the VCO is tracking the DDS. The error is normally zero except at the slope transitions when the error briefly spikes but remains less than 180º, monotonic and non-saturated.

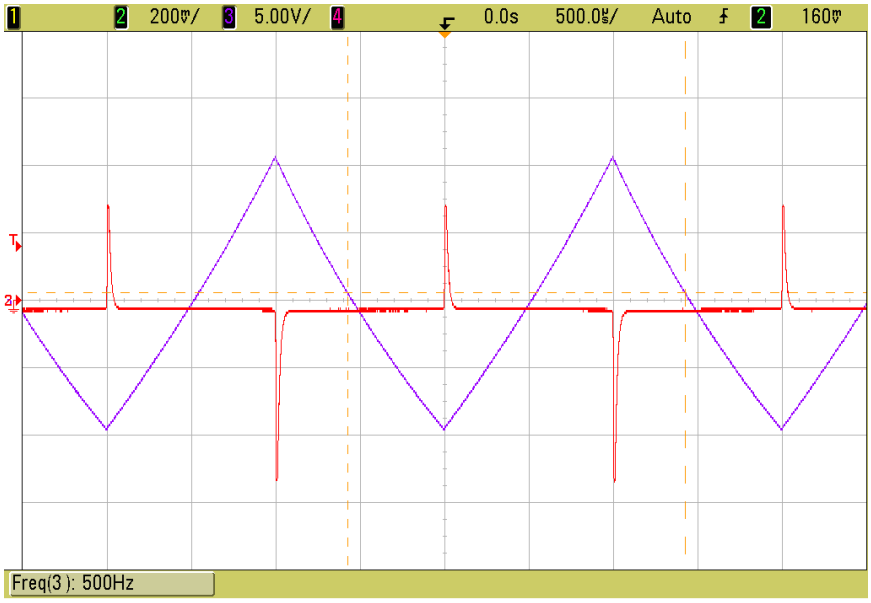


Figure 11 VCO Control Voltage and Loop Error Voltage

mmWave Radar System

The hybrid synthesiser module has been built into a short range instrumentation RADAR incorporating a further x4 frequency multiplier to reach 75 GHz with a 6 GHz bandwidth. The return signals are processed using a custom DSP based FFT processor.

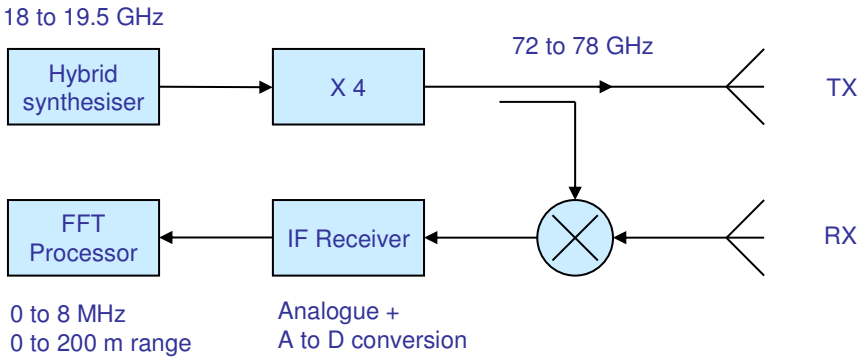


Figure 12 mmWave Radar System

A simple laboratory test was carried out with a metal target placed on a particle board and foam support table. An example response is shown in Figure 13. The test target return can be clearly identified at 1904 cm. Also clearly visible are returns from the front and back edges of the support structure at around 1870 and 1944 cm.

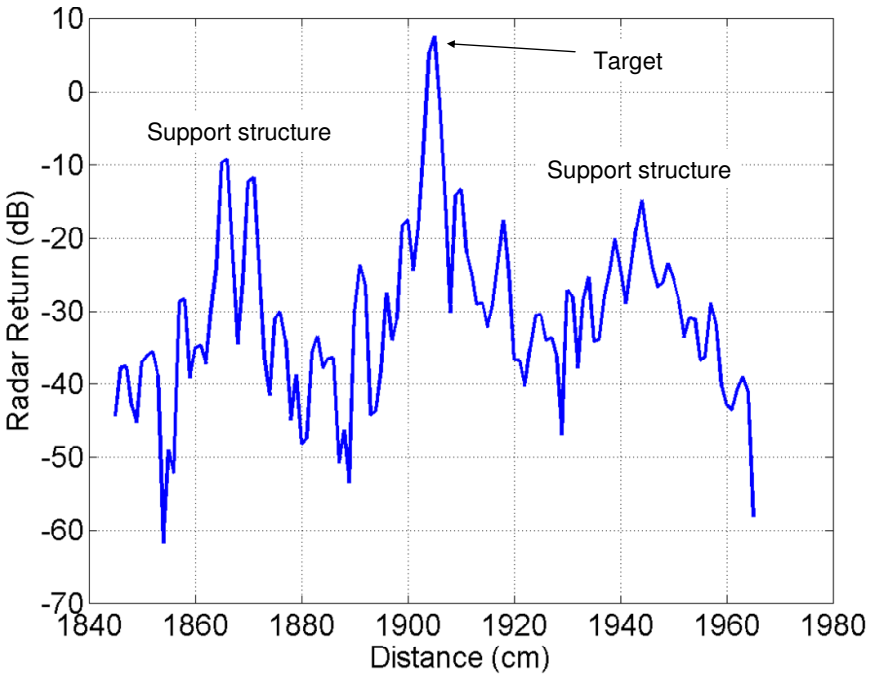


Figure 13 Typical Target Return

Conclusions

The PLL/DDS Hybrid Synthesiser has demonstrated excellent performance:

High linearity	:	<< 0.01% (from RADAR results; not directly measured)
Low spurious levels	:	< -80dBc typical
Flexible Architecture	:	Independence of bandwidth and centre frequency
Re-configurable	:	digitally programmable in real time (within constraints)
No calibration	:	closed loop, feedback system

Acknowledgements

The authors would like to thank Cobham Technical Services for supporting and funding the development of this system.