GaN Technologies
Applications, Status and Trends

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***Abstract*— GaN technology has gained a lot of attention in Europe over the last few years for various domains including RF electronics. This paper presents a brief summary and the current status achieved on GaN technologies in Europe in comparison to the competition around the world. Aspects covering material, devices up to circuits and module integration is addressed. Two technologies associated to gate length of 0.5µm and 0.25µm have been identified covering respectively applications up to 7 GHz (transistors and power bars) and MMICs up to 20 GHz.**

State of the art results from L to C bands on elementary power transistors and power bars (Radar, telecom) and preliminary results in X-Band and Wideband applications for Radar and EW applications. Some elements of reliability will be also given, summarizing the current status and key challenges on which progress is expected.

I. Introduction

ALGAN-GAN HEMTs are of particular interest for RF applications due to their high-electron mobility, large breakdown electric field, and good thermal stability. Since the first demonstration of AlGaN/GaN HEMTs in 1993 [1], great microwave power performance [2] has already been achieved, because of many breakthroughs obtained in growth [3], device designs [4], [5], and processing [6]. For millimeter-wave applications, from Ka-band up to W band AlGaN / GaN HEMTS also exhibits very promising results [7-8] and seems to be an opportunity to extend the power capabilities of this technology.

Over the last years the focus has strongly shifted to GaN-based devices and a large community including Academia, Industry and National research institutes is now strongly involved in the development of GaN devices and technology. Although in the last decade Japan and the US have mostly been in the limelight, in particular with the first products being put on the market, significant and innovative work has also been done in Europe reaching to the state-of-the-art. The paper will try to summarize and draw a picture of the current status of the GaN technology in Europe and the perspective for the years to come. The content will try to cover all topics from material to modules for RF-applications.

Since a few years the GaN activity in Europe has dramatically increased. This activity is solidly based on a few important cornerstones:

- A long and extensive experience of III-V semiconductors and RF applications in the Academia as well as the Industry. For most players the transition from GaAs to GaN was a logical move.
- A strong commitment from the industry that recognized that its future would be increasingly dependent on GaN technology even if GaAs remains a major player for many years to come.
- The awareness of the European institutions that the GaN technology would become a key enabling technology for many applications and that without it Europe would lose its independence and competitiveness and many industrial and strategic areas. In consequence, many projects were initiated to support and push the development forwards. All domains are being addressed including Space, Commercial and Defence.

II. Contracts &Technological Roadmap

Thanks to the support of contracts from European agencies, National agencies and specific supports, GaN HEMT technologies are on the right track to be industrialized in Europe offering a very competitive alternative to US and Asian competition. Two federating projects we could mention is “Korrigan” [9,10] (supported by the European Defence Agency, or EDA), that covers all aspects from Substrates to Modules; or “GREAT$_2$“ [11] (supported by the European Space Agency, or ESA), that focuses on reliability improvement for

Space applications. Supports from French (DGA) and German (BWB) MoDs, CNES, DLR, ANR, BMBF, and EADS, Thales participate to accelerate the development of GaN technologies through different cooperative programs. We note also that UMS uses the support of two major laboratories in Europe : IAF[12] and Alcatel-Thales III-V lab. [13] GaN technology needs a strong commercial basis to survive and expend. The base station (BTS) market represents good opportunities, especially for future wideband standards and multi-standard products. As a major player in this field, NXP has planned the introduction of GaN RF power transistors for the next year in partnership with UMS, through a dedicated development program also involving the Fraunhofer Institute for Applied Solid-States Physics (IAF) and Chalmers University [14].

To support all these programs, UMS has defined a very aggressive technological roadmap which stays relatively unchanged since one-year.

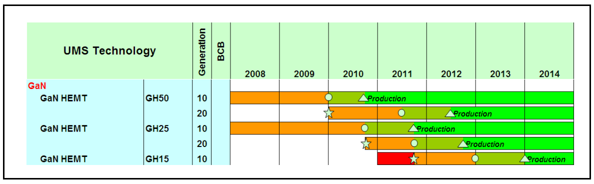

Figure 1 : Technological GaN HEMT Roadmap

The GH50 (0.5µm gate length) technology will cover applications up to 7 GHz. First version, ie GH50_10, planned to be qualified in 2010. It will propose elementary transistors and power bars for BTS, Radar (L to C bands), wideband for EW/Jamming and SSPA for Satcom applications. The GH25 (0.25µm gate length) technology will be available in 2011 for applications ranging from 4 to 20 GHz and propose a complete set for MMICs design or hybrid development. Applications like Radar, EW and SSPA for Satcom applications in Ku band are targeted. Specific high power development are also aimed for TWT replacement.

III. GaN HEMT Technology

The AlGaN/GaN technologies are developed entirely with the UMS process on 3-inch and 5-inch GaN on SiC wafers. Two processes, GH50 and GH25, are developed in parallel with the maximum of synergy regarding the process modules. The epitaxial structure has a SI GaN buffer with advanced Fe-doping for improved isolation. The AlGaN schottky barrier layer is optimised respectively for the RF performances, robustness and reliability aspects.

The active device epitaxial layers were isolated by implantation. The ohmic source-drain spacing was ranging from 2 to 4-µm with nominal contact resistance of 0.5Ω-mm. The gate-length was defined by patterning and etching a 0.5 or 0.25-µm opening in the SiNx respectively for GH50 and GH25. A second patterning and subsequent metallization over the etched SiNx opening completes the gate metal and forms an integrated field-plate. In addition, a source-connected second field-plate (2FP) was implemented to reduce the electric field and improve the reliability. Both field-plate are optimised to reduce the parasitic coupling (feedback capacitance) and thus to improve the PAE and gain at high voltage. For backside via, the SiC wafers were ground andpolished to 100-µm, and the GaN/SiC vias were etched in an ICP-RIE process. Finally, the backside ground plane was plated with > 4-µm of Au.

The DC transfer characteristics are measured at VDS = 10V and 40V and VGS = -7V to 1.5V. Median threshold voltage was -2.5V for GH25 and -2.0V for GH50. The maximum dc transconductance was in excess of 350mS/mm for GH25 and 200mS/mm for GH50.

Maximum drain current at Vgs = 1.0V was 1.0A/mm or 0.65 A/mm respectively for GH25 and GH50. The reverse breakdown voltage was greater than 150V or 200V for IGD =1mA/mm. respectively for GH25 and GH50.

IV. Reliability - preliminary

Preliminary strategy of test consists to evaluate the Absolute Maximum Ratings (AMR) of the technology. Again, these limits during the technological development could evaluate versus the technological iterations. It consists in :

- DC step stress : HTRB and HTOL test are recorded respectively by steps of 5V to 10V on Vds, and 10% on IdQ with a period of 168 hrs.
- RF step stress : by steps of 5V on Vds with an increasing compression of 1 dB and with a period of 168 hrs.

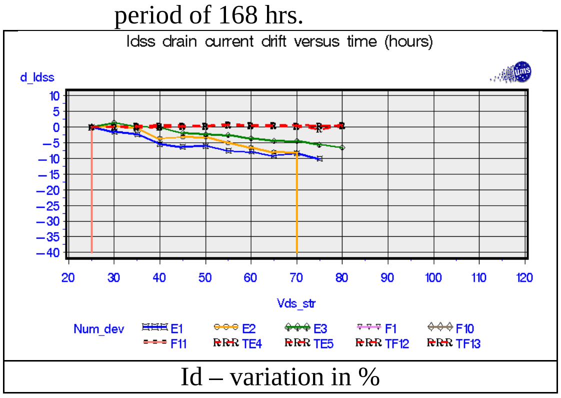

Figure 2 : DC step stress on a 0.25 µm GaN HEMT transistor. Tc=Tambient.

The following list of test is identified to identify the main mechanisms (Ea) of degradation and used after to qualify the technology demonstrating the MTTF limitation:

- HTRB (High Temperature Reversed Blocking) : this test has to evaluate the sensitivity to high voltage, high temperature.
- HTOL / IdQ (High Temperature Operating Life test / Quiescent Drain current test) : definitions very close. This test is performed at Vds_0 and Idss x 0.01 < Ids_0 < Idss x 0.5 corresponding respectively to deep AB or AB class biasing current.
- RFLT (RF life test) : CW life test are recommended to capitalize a lot of hours. These tests are performed on the basic power cells representative of the technology (10 W to 20 W from 1 to 6 GHz down to 5W for X or Ku bands).

The [Figure 3] gives a representation of long term measurement (HTRB) measured at 30V on the 0.25µm gate process after 8000 hours of aging tests without failure.

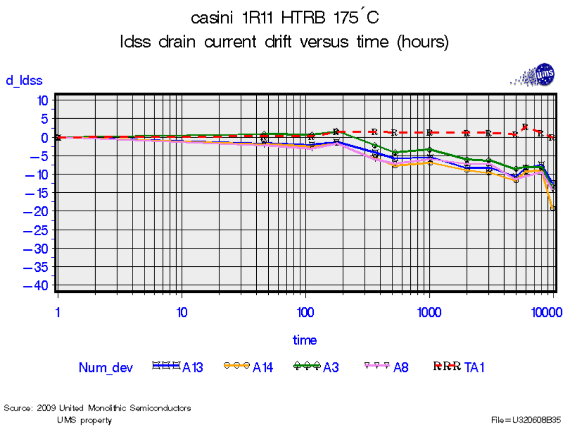

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Figure 3 : HTRB test performed at Vds=30V – Tc = 175°C – transistor of 1mm gate development device (8x125µm)

V. GaN HEMT : RF performances

V.1. GH50

Different characterizations have been performed to optimise the topology of the gate module which is critical to get high performance. The following figure gives the compromise between Output power and PAE optimum loads (field plates topology). All these characterizations are done at 3.3 GHz on a 3.2mm of gate development (8x400µm) – Vds=50V – pulsed mode (500µs pulse length – 15% Duty cycle). A PAE above 55% associated to 6W/mm is easily obtained for a condition corresponding to the maximum of power.

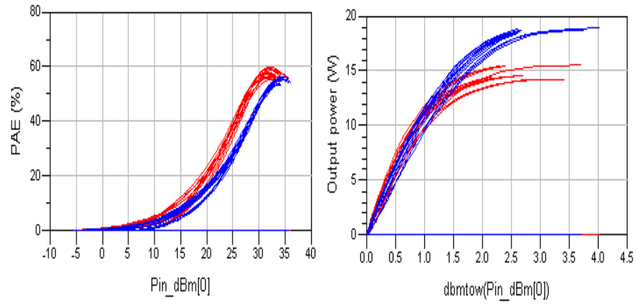


Figure 4 : On-Wafer Load-pull characterizations – Vds=50V – pulsed mode – f=3.3 GHz

Specific architecture of transistor have been designed to address the need for C-Band or very wideband application. The next figure gives a result obtained at 6 GHz on a 2 mm device (8x250µm) – Vds=50V in pulsed mode. Again, compromises between power and PAE in term of optimum loads are shown (blue and red curves).

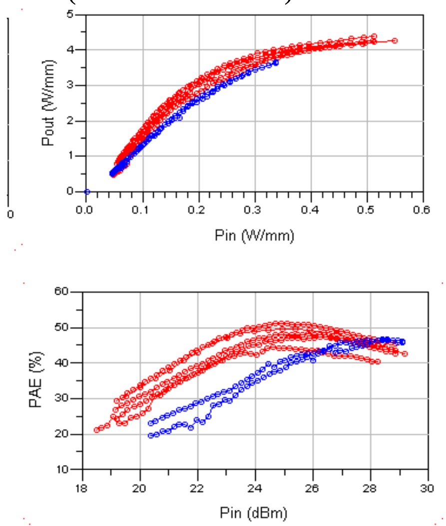
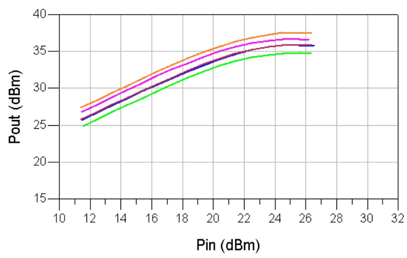


Figure 5 : On-Wafer Load-pull characterizations – Vds=50V – pulsed mode – 6 GHz

V.2. GH25

A lot of characterizations have been performed to optimise the epitaxy associated to the gate module to optimise the performances up to 18 GHz. The following figure gives the dependence versus Vds from 25 to 50V. All these characterizations are done at 10 GHz on a 0.6 mm of gate development (8x75µm) –pulsed mode (10µs pulse length – 10% Duty cycle). From the figure, we observe 9W/mm associated to more than 55% PAE at Vds=50V.



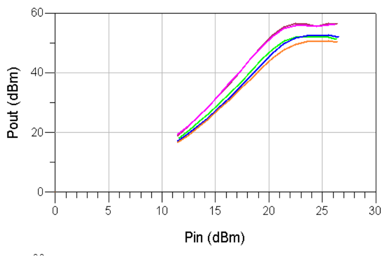


Figure 6 : On-Wafer Load-pull characterizations – Vds=25V(green) to 50V (orange) – pulsed mode – 10 GHz

VI. GaN HEMT : Circuit performances

A monolithic three stage high power amplifier (HPA) has been developed for wide band applications. This amplifier is fabricated on UMS 0.25 µm GaN on SiC device technology (GH25). The MMIC HPA provides in continuous-wave (CW) mode 6 to 10 W output power from 6 to 18 GHz with power added efficiency from 14 to 25% and minimum small signal gain of 18 dB. The main measurement results in test fixture in CW mode at Vds=25V are illustrated in the following curves:

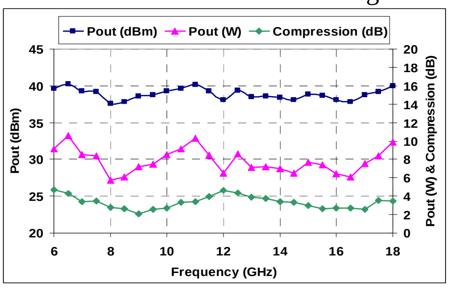


Figure 7 : CW Output Power and Gain compression at Pin=22dBm

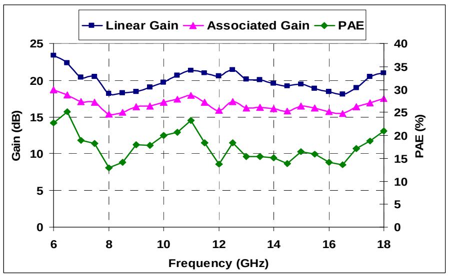


Figure 8 : CW Pae at Pin=22dBm, associated and linear Gain

GH50 technology is developed to address high power applications (wide band, narrow band, from L to C-band). Different topologies of power bars have been designed highlighting the needs to address very wideband applications. Several products are under development in RF power packages for S, C and wide band applications.

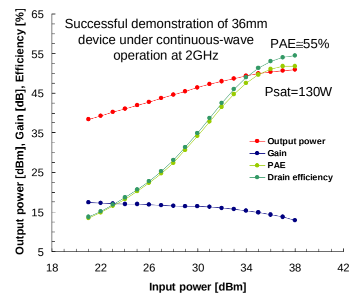


Figure 9 : Left: L-Band power bar load pull result (Courtesy of NXP)

VII. CONCLUSION

UMS has developed two families of GaN technologies for application between 2 and 20GHz with state-of-the-art performances. The first generation is due to be qualified in 2010 and 2011 for half- and quarter-micron gate-length devices respectively. In both cases, first demonstrators have been designed and fabricated already that demonstrate the performances achieved. Further generations are planned later with improved performances and features. Additionally, at two more families are planned to address higher frequencies and specific applications respectively.

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