

A New Frequency Synthesiser for Commercial Satellite Communications in Ku-Band.

A. David Williams

Teledyne Microwave
1274 Terra Bella Avenue
Mountain View
California 94043
USA

Abstract— This paper describes a new Frequency Synthesiser design in Ku-Band. The design uses a single microwave Phase Locked Loop which includes a novel phase comparator circuit.

I. INTRODUCTION

The INTELSAT IESS standards for commercial satellite communications equipment define the frequency accuracy, channel allocations and spectral purity requirements for Earth Station Transmitters.

Earth station transmission equipment commonly makes use of single or dual frequency conversion processes with a Frequency Synthesiser providing the final Local Oscillator tuneable in steps of 1 kHz.

Historically Frequency Synthesisers of this type were designed with multiple Phase Locked Loops often using the "Mix and Divide" process. [1]

This paper describes a new Frequency Synthesiser design using a single microwave PLL which includes a "Compound Phase Detector" (Patent Pending).

II. DISCUSSION

A. Historical Perspective.

Historically designers often made use of the "mix and divide" process as shown in Figure 1 in order to achieve small frequency step size

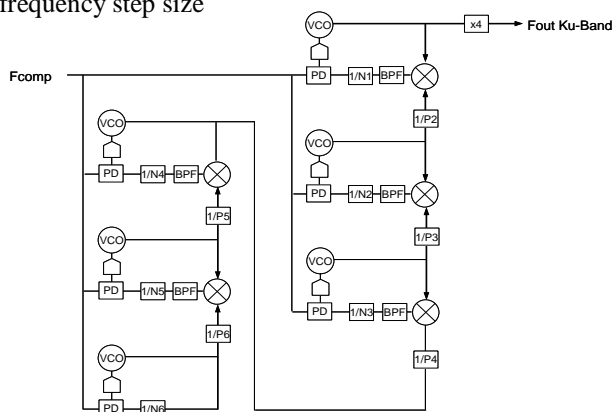


Figure 1. Mix and Divide Frequency Synthesiser.

This technique involves the use of a number of cascaded PLLs with frequency summation mixers and is capable of moderate phase noise performance mainly dominated by the primary PLL since the "vernier" PLLs only need to tune over a frequency range equal to $P \times$ (Primary PLL step size).

However Frequency Synthesisers using this technique were complex, large and expensive; they were also difficult to realise because of their stringent filter requirements.

Fractional-N PLL technology appeared in the early 1980s [2], [3] allowing Frequency Synthesiser designers to produce devices having small output frequency steps using fewer PLLs. However designs based on this technique are very prone to generating spurious output signals.

B. DDS Techniques

Direct Digital Frequency Synthesiser (DDS) devices became available in the late 1980s (Plessey Semiconductors SP2002 for example), providing designers with a means of generating high frequency signals (realistically up to around 100 MHz) tuneable in extremely small steps (step size = clock frequency / accumulator capacity). A modern 48 BIT DDS clocked at 1 GHz will have a minimum step size of: $10^9 / 2^{48}$ Hz $\sim 3.6 \mu\text{Hz}$.

DDS and Integer-N PLL technology may be combined in Microwave Frequency Synthesizers using the "DDS Tracking PLL" shown in Figure 2.

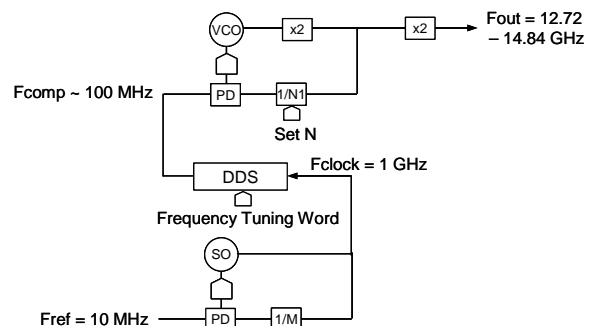


Figure 2. DDS Tracking PLL.

DDS Tracking PLL frequency Synthesisers require more complex programming methods, since setting the output frequency involves some calculation:

Referring to Fig 2.

If $F_{comp} \sim 100$ MHz then set $N = \text{FLOOR}(F_{out} / 2 \times 100)$.

If F_{out} is required to be 12756.003 MHz then N will be given by $\text{FLOOR}(12756.003 / 200) = 63$.

If N is now set to 63, F_{comp} will need to be set to $(12756.003 / 2 \times 63)$ MHz = 101.238119 MHz.

If a 48 BIT DDS is used clocked at 1 GHz, the Frequency Tuning Word (FTW) will need to be set to:

$$101.238119 \times 2^{48} / 1000 = 2.84959972 \times 10^{12}$$

This may be represented as a 6 byte Hexadecimal number equal to: 02 97 79 61 0a 40 hex

The calculation may be performed in a microcontroller, but the process will be slow (~ 100 milliseconds). Alternatively a high speed microprocessor (ARM 7 or similar) may be used, in which case the calculation may be completed in a few hundred microseconds.

C. Phase Noise Considerations.

The Phase Noise performance of any single loop Frequency Synthesiser is controlled by the following factors:

1. Output Frequency
2. Crystal Reference Oscillator Phase Noise
3. Phase Comparison Frequency (F_{comp})
4. Phase Detector Noise Floor
5. VCO Phase Noise
6. Loop Division Ratio N .
7. Output Frequency Multiplier.

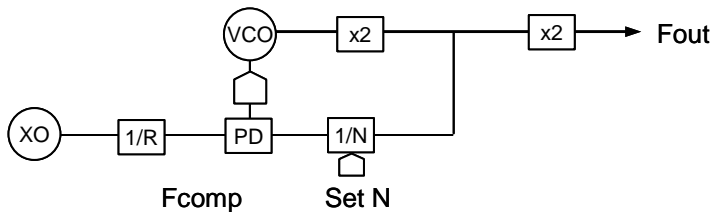


Figure 3. Simplified Single loop Frequency Synthesiser.

If we assume the following parameters are set in Figure 3 above:

1. Output Frequency = 10 GHz
2. Crystal Oscillator Frequency = 100 MHz.
3. Phase Comparison Frequency = 10 MHz
4. VCO Frequency = 2.5 GHz
5. Loop Division Ratio = 500
6. Output Frequency multiplier = 2x

The phase noise plateau level at output frequency F ($PCNF_F$), at carrier offset frequencies less than the PLL Loop Bandwidth will be given by:

$$PCNF_F (dBc/Hz) = PCNF_{ABS} + 10\log(F_{comp}) + 20\log N + 6$$

Modern PLL controller ICs, such as Analog Devices ADF 4106, display $PCNF_{ABS}$ values around -219dBc/Hz (Referred to 1 Hz) The in band phase noise plateau of the circuit in Figure 3 will therefore be approximately equal to $-219 + 70 + 54 + 6 = -89$ dBc/Hz.

The output frequency for this circuit will be given by the equation:

$$F_{OUT} = 2 \times N \times F_{comp}$$

The output frequency step size will be:

$$dF_{OUT} / dN = 2 \times F_{comp}$$

It can be seen that, in order to produce small output frequency steps, F_{comp} must decrease and N must increase with a consequent lifting of the $PCNF$ plateau level.

From the above discussion, it should be apparent that the DDS Tracking PLL technique becomes very attractive when small output frequency steps are required.

D. Phase / frequency comparators

1) Digital devices

As described above, the main factor limiting the phase noise performance in a single PLL is the $PCNF$ of the phase comparator at any given comparison frequency F_{comp} . Sequential digital phase / frequency comparators often employ two flip-flops and a NAND gate, as shown in Figure 4.

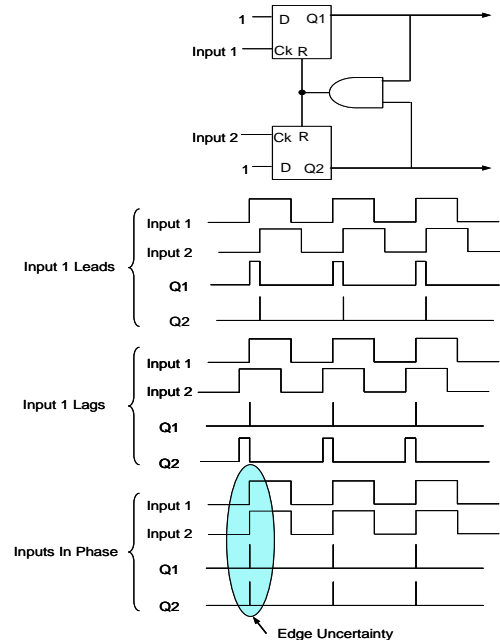


Figure 4. Sequential Phase / Frequency Comparator.

The two output signals from the Phase / Frequency comparator are often fed to the differential inputs of an active low pass filter built around a low noise Operational Amplifier. In the locked condition, the divided VCO signal will be In Phase with the reference signal.

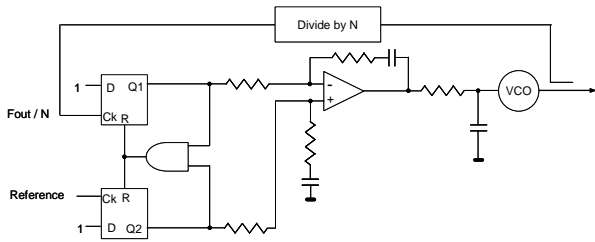


Figure 5. PLL using a sequential phase comparator.

Sequential Phase Frequency Comparators are in common use and exhibit very good PCNF performance; a very attractive characteristic of these circuits is their ability to sense frequency as well as phase.

The major factor limiting the noise floor of sequential phase comparators is "edge uncertainty" when the device is used to lock a divided VCO signal to a reference signal.

The flip-flops and gate exhibit finite rise and fall times on their output signals and there is also a finite delay associated with the reset function in each flip-flop.

Motorola introduced the MC4044 TTL phase comparator in the 1970s with an absolute PCNF around -205 dBc/Hz. Motorola introduced the ECL based MC12040 soon after, which was capable of performing phase comparisons up to about 80 MHz, however the PCNF of this device was similar to the MC4044 because of the increased noise levels in the ECL gates and flip-flops.

It is interesting to note that a similar situation exists today. Sequential phase comparators built using GaAs Heterojunction Bipolar Transistor (HBT) technology are commercially available; these devices are capable of performing phase comparisons up to 1.3 GHz. However their PCNF is around -217 dBc /Hz, again because of flicker noise generated in the gate and flip-flops.

2) Analogue Phase Comparators.

If two signals at the same frequency are fed to an Analog Multiplier device it becomes a Phase Comparator due to the convenient trigonometric identity:

$$\int_{\omega t=0}^{\omega t=2\pi} A \sin \omega t \times B \sin(\omega t + \phi) = AB \pi \cos \phi$$

where A and B represent the peak amplitude of each signal and ϕ represents the phase difference between the two signals.

If the value of this function is plotted versus ϕ over the range 0 to π , a characteristic "S Curve" is produced, which passes through zero volts output when $\phi = \pi/2$.

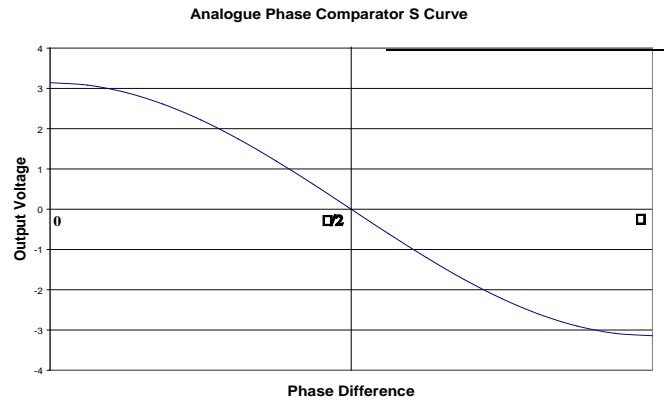


Figure 6. Analogue Phase Comparator S Curve.

NOTE: Diode Ring Multipliers (Double Balanced Mixers) exhibit a negative polarity S Curve.

Analogue Phase Comparators generally exhibit superior PCNF performance compared with digital devices (PCNF for an APC is approximately -230 dBc/Hz) [4], [5], [6]. However they suffer from the limitation that they cannot detect frequency difference. Consequently, conventional PLLs containing Analogue Phase Comparators require some form of acquisition circuit to bring them into lock.

III. A COMPOSITE PHASE FREQUENCY COMPARATOR

Referring back to Figure 5:

When the PLL is locked the reference and divided inputs to the phase comparator will be maintained in the "in phase" condition. If now the reference input is split into two paths and a 90° phase shifter is inserted into the second path it becomes possible to connect an auxiliary Analogue Phase Comparator (APC) in parallel with the sequential phase comparator, since the input signals to the APC will be in quadrature.

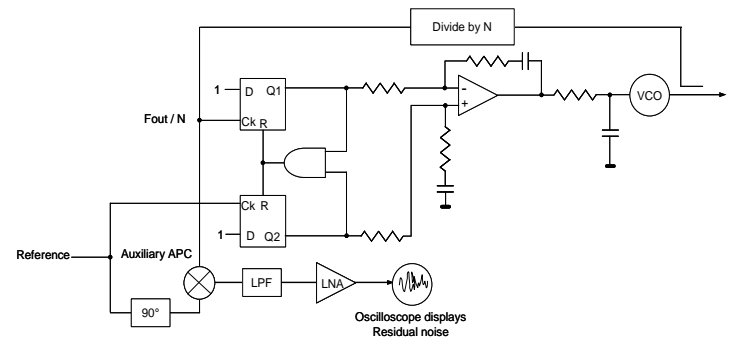


Figure 7. PLL with an auxiliary Analogue Phase Comparator.

The output signal from the auxiliary APC has two components; the first being a signal at twice the phase comparison frequency and the second representing phase fluctuations (noise) which have not been resolved by the sequential phase comparator.

The high frequency component of the APC output may be removed by filtering and the noise component may be amplified by a Low Noise Amplifier and displayed on an oscilloscope. See figure 8 below.

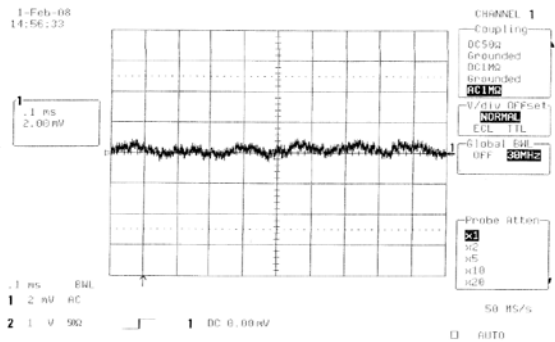


Figure 8. Phase Comparator Residual Noise (2mV/Divn).

The technique described above was originally devised to test phase comparators however it became the basis of the design for a new Frequency Synthesiser.

(U.S. Patent Application No. 11/803,602. May 15th 2007)

IV. A Ku-BAND FREQUENCY SYNTHESISER

It became apparent that the residual noise resolved by an auxiliary APD could be fed back into the PLL loop amplifier in such a way as to improve the overall PCNF in the loop.

The composite phase comparator has been incorporated into the Frequency Synthesiser shown in Figure 9.

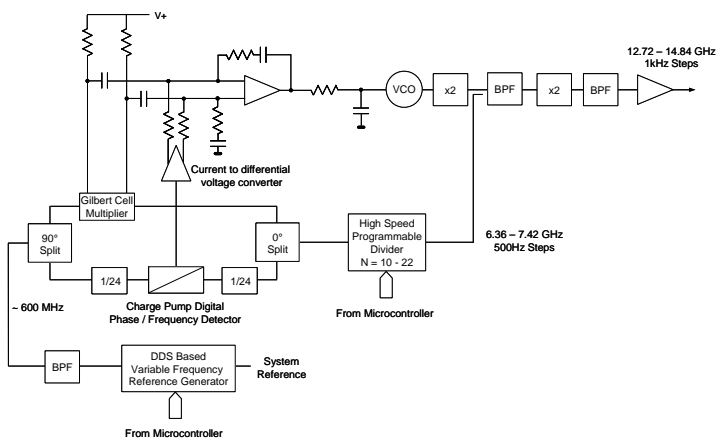


Figure 9. Ku-Band Frequency Synthesiser.

A VCO operating in S-band drives a frequency multiplier chain to provide output signals in the range 12.72 – 14.84 GHz. A sample of the doubled VCO signal is fed to a high speed programmable divider via a directional coupler; the divider may be set to any integer value between 10 and 22.

A phase comparison frequency of approximately 600 MHz is used and the loop division ratio is determined using the method described in section B of this paper.

The composite Phase / Frequency comparator comprises a Sequential Phase / Frequency comparator driven at $(F_{comp} / 24)$ and a Gilbert Cell Multiplier driven directly at F_{comp} .

Reference signals are fed to the two Phase Comparators in quadrature through a 90° power divider.

The $1/24$ fixed dividers in each input arm of the sequential phase comparator are identical and therefore introduce similar amounts of time delay (phase shift).

The sequential Phase Detector and one $1/24$ divider reside within a commercial PLL controller IC (Analog Devices ADF4106); the second $1/24$ divider resides in a second ADF4106 device. The sequential phase /frequency comparator has a Charge Pump output stage; a current to differential voltage converter circuit is used to generate a differential voltage to drive a third order, active loop filter.

The loop filter output drives the VCO tuning port thereby closing the Phase Locked Loop.

When the PLL is locked, the input signals to the sequential phase comparator will be in phase, as will the input signals to the two $1/24$ dividers; the input signals to the analogue phase comparator (Gilbert Cell) will be in phase quadrature.

The differential output signal from the Gilbert Cell represents the residual loop noise below the Noise Floor of the sequential phase comparator; these signals are capacitively coupled to the input of the loop filter.

The sensitivity of the analogue phase comparator (volts/radian) is much greater than that of the sequential phase detector; (typically $K\phi = 4$ volts/radian for the APC compared with 0.05 volts/radian for the sequential phase comparator / divider combination) consequently the APC dominates the PLL noise performance at offset frequencies greater than the cut off frequency of the capacitive coupling network.

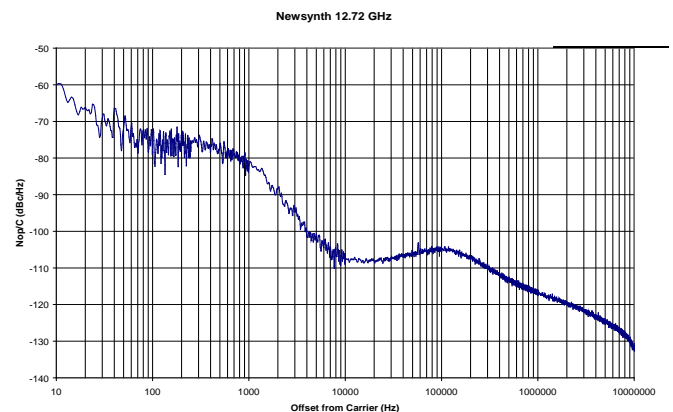


Figure 10. Ku-Band Frequency Synthesiser Phase Noise Plot.

The phase noise performance of the Ku-Band Frequency Synthesizer has been measured using an Agilent E5503B Phase Noise Analyser system and is shown in Figure 10 above. The SSB phase noise to carrier ratio at 10 kHz offset from the carrier is approximately -109 dBc/Hz at an output frequency of 12.72 GHz.

The Frequency Synthesiser exhibits RMS Phase Jitter of approximately 0.4 degrees and a DSB carrier to Noise Ratio of 43 dB over the offset range 100 Hz to 1 MHz.

The author believes this performance represents the current state of the art.

V. CONCLUSION

A new Frequency Synthesiser operating in Ku-Band has been developed; the device makes use of a composite Phase / Frequency Comparator and Direct Digital Synthesiser technology.

The Frequency Synthesiser is shown in Figure 11; the device is built on an eight layer, composite dielectric PCB 200mm x 125 mm.

REFERENCES

- [1] F. M. Gardner, *Phaselock Techniques*, 3rd ed. John Wiley & Sons Inc, New York 2005.
- [2] G. G. Gillette, "Digiphase Principle" *Frequency Technology*, August 1969.
- [3] U.S. Patent 3,959,737, Frequency Synthesiser Having Fractional Frequency Divider in Phase Locked Loop, W. J. Tanis, Engelmann Microwave, Montville New Jersey, May 25th, 1976.
- [4] J. A Crawford. "*Frequency Synthesizer Design Handbook*" Artech House 1994.
- [5] F. L Walls, S. R Stein, "*Accurate Measurements of Spectral Density in Devices*" 31st Annual Frequency Control Symposium. 1977
- [6] M.C Fischer "*Frequency Domain Measuring Systems*" 10th Annual Precise Time and Time Interval Applications and Planning Meeting, December 1978

The Frequency Synthesizer may be tuned in frequency steps of less than 1 Hz and exhibits very low levels of phase noise at its output.



Figure 11. Ku-Band Frequency Synthesiser PCB.