Intrinsic Cree GaN HEMT Models allow more accurate waveform engineered PA designs
Ray Pengelly and Bill Pribble, Cree RF Products
April, 2013
Summary

• Advantages of GaN HEMT Technology
• Overview of Large-Signal GaN HEMT Models
• Waveform Engineering of GaN HEMT PA’s
  ❑ Actual Current Generator and Drain Voltage Waveforms
• Example of Harmonically terminated narrow band PA
  ❑ Effect of parasitics in packaged transistors on true device waveforms
• Example of Determining VSWR Robustness for a Single-Ended PA
• Example of Class F Doherty PA
  ❑ Carrier and Peaker Waveforms/Load-lines at Crest and 7.5 dB OBO
• Conclusions
Advantages of GaN HEMT Technology
Summary of GaN HEMT Advantages

• Wide bandgap semiconductor materials like GaN HEMTs have potential to operate at power densities many times higher than Si-LDMOS, GaAs FET, and silicon carbide (SiC) devices

• High power density is an important factor for high power devices enabling smaller die sizes and more easily realized input and output matching networks

• GaN HEMTs have other advantages:
  – High breakdown voltages (200+ volts)
  – High saturated electron velocity
  – Good thermal conductivity
  – Low parasitic capacitances and low turn-on resistances
  – High cut off frequencies

• Proven high reliability (>10 million hours) and excellent field FIT rates (<10)
MTTF at 225 deg C Channel Temperature is >20 million hours

Most GaN transistors are specified to withstand a 10:1 output mismatch at fully rated output power. Worst case in example above shows PAE of 7% and a maximum channel temperature of 278°C but device does not fail
Overview of Cree Large-Signal GaN HEMT Models
Large signal models are available for all Cree GaN HEMT transistors
  - Agilent’s ADS and AWR’s Microwave Office are fully supported
Highly accurate with excellent history of design pass successes
Enable complete DC and RF simulations
Models include self-heating (presently single-pole thermal time constant)
Model library is regularly updated
Latest model library revision uses Verilog A code and includes 0.4μm and 0.25μm gate length transistor models
6 port capability is being added to all models so that true “intrinsic” drain currents and voltages at the current generator are available
  - In addition $C_{DS}$ and package parasitics are “removed”
Many marketing reference designs can be provided
Models for GaN HEMTs

- Equivalent-circuit based approach
  - Relatively simple extraction
  - Process sensitive based on individual elements
  - Simple implementation using commercial harmonic balance simulators
- Significant historical information for model basis and validation
- Non-linearity introduced as required by element
  - Drain current source is dominant non-linearity
  - Gate current formulation includes breakdown and forward conduction
  - Voltage variations of parasitic capacitances derived from charge formulations
- Model data fit extends over drive, frequency, bias, and temperature
- Many hundreds of successful hybrid and MMIC designs
Based on 13-element MESFET model (Fager-Statz)

ADS version shown using non-linear equation-based elements
• Most FET models implement a gate current-control characteristic that transitions from the sub-threshold region to the linear gate control region directly, without treating the intermediate region, called the quadratic region. Fager et al. implemented an equation and new parameters to fit the quadratic region. This leads to better agreement with measured IMD and other nonlinear characteristics.

• Gate charge is partitioned into gate-source and gate-drain charge. Each charge expression is a function of both $V_{DS}$ and $V_{GS}$. Using charge partitioning, it is possible to fit most GaN HEMT capacitance functions and observed charge conservation.
The model includes new capacitance functions as well as modeling of the drain-source breakdown and self heating.

The model has four ports, with the extra port providing a measure of the temperature rise. The voltage between the external thermal circuit port and the source node is numerically equal to the junction temperature rise in degrees C. This occurs because the current source in the thermal circuit is numerically equal to the instantaneous power dissipated in the FET and the resistance, $R_{TH}$ is numerically equal to the thermal resistance. The RC product of the thermal circuit is the thermal time constant.

The model addresses the sharp turn-on knee in GaN HEMTs leading to the accurate prediction of IMD sweet spots in Class A/B operation.
Temperature Dependence – Self-heating

- Drain current is only temperature dependent model element
- Drain current scales to provide -0.1 dB/10°C reduction in power for current-limited load-line
- Self-heating included using a thermal resistance – calculated from finite element analysis of die and package.
- Thermal performance due to package needs to be included where appropriate
- Feedback capacitance is a strong function of drain voltage
- Inclusion of this effect necessary to fit small-signal data
- Non-linearity changes harmonic generation from the model – effects efficiency and linearity predictions
- Output Capacitance $C_{DS}$ is linear – no voltage dependence (weak anyway)
• Input capacitance is a strong function of gate voltage
• $C_{GS}$ is also a function of drain voltage, but this non-linearity is not included at present
• The gate-voltage non-linearity also affects model’s harmonic generation
On-wafer S-parameters of 0.5 mm HEMT – 25°C baseplate
Major challenge of modeling for high power circuits – scaling from reasonable test cell to large periphery output stages – successfully implemented for scaling factors >100:1
Non-linear model fits small-signal parameters over a range of bias voltages
All measurements performed using 1% duty cycle, 20µs pulsed bias to control thermal effects
GaN HEMT Model - Large-Signal

- On-wafer load-pull of 0.5 mm HEMT
- Measured at 3.5 GHz, \( V_{DS} = 28 \) V, \( I_d \sim 25\% I_{DSS} \), 25°C chuck temperature
- PAE contours not used for modeling due to sensitivity to harmonic loading
  - PAE verified using hybrid amplifier measurements
Waveform Engineering of GaN HEMT PA’s
• Depending on the Class of amplifier being designed the drain voltage and current waveforms of an RF driven GaN HEMT need to be in exact anti-phase for maximum DC to RF conversion efficiency

• In many cases optimum efficiency will be provided when the voltage is a square wave and the current is a half sine-wave in anti-phase (Class F) or the voltage is a half sine-wave and the current is an anti-phase square wave (inverse Class F)

• Perfect half-sinusoids and square waves require an infinite number of signal harmonics

• Practically 3 harmonics is a limit both from device physics as well as amplifier realization viewpoints
Waveforms at the Current Generator Plane

• In many cases where packaged GaN HEMTs are being employed in PA designs the waveforms presented at the package planes DO NOT REPRESENT the waveforms at the actual transistor current generator
  – Package parasitics etc. effectively provide impedance transformation and phasing networks (with their own losses etc.) to the true transistor current generator plane.
  – Attempts (some successful) have been made to “de-embed” package equivalent circuits, die level capacitive parasitics etc. from the large-signal models provided by some of the GaN HEMT vendors
  – Cree is now deploying new large-signal transistor models, with a total of 6 ports (gate, drain, source, current generator, drain voltage and channel temperature sense) providing a true “intrinsic” model
Example of Harmonically Terminated Narrow Band PA
High Efficiency S-Band Radar PA

- 3 Harmonic Tuned 120 watt PA utilizing Cree CGH40120F packaged transistor
- Ideal harmonic tuners used on input and output of device. Quiescent Drain Current set to 1A at a drain voltage of 28 volts
- “Intrinsic” 6 port model used
Comparison of Waveforms at “correct” and “incorrect” reference planes

Extrinsic Waveforms

Intrinsic Waveforms

Note current goes to -4.2A at package planes!

Intrinsic current is close to zero at minimum!

Dynamic Load Line at full output power

Greater than 80% efficiency

Copyright © 2013, Cree, Inc.
Example of Determining VSWR Robustness for a Single-Ended PA
- There are three major reasons why GaN HEMTs may fail under VSWR Mismatch conditions
  - Excessive RF Drain Voltage
  - Excessive RF Drain Current
  - Excessive Channel Temperature
- As will be shown in the following example a nominal 28 volt GaN transistor (CGH40025F) operated into a 10:1 VSWR (any phase) can have an instantaneous drain voltage (at the die level) that exceeds 100 volts.
  - Clearly the relevant technology needs to support a typical drain breakdown voltage of 120 to 150 volts
Output VSWR Robustness (1) – Drain Voltage and Current

5:1 VSWR Peak Drain Voltage = 93 volts (Vds=28 volts)

10:1 VSWR Peak Drain Voltage = 105 volts (Vds=28 volts)
Cree GaN HEMT Maximum Channel Temperature is recommended at 225°C. So under 10:1 VSWR maximum case temperature should not exceed 65°C at continuous full output power.
Example of Class F Doherty PA
• Unequal split two-way Doherty
• Employs two CGH40010F transistors
• 5 watts Pave at 7.5 dB OBO
  • Ideal for Small Cell Telecoms
• > 56% drain efficiency with 18 dB gain at 2.14 GHz
• Each amplifier (main and peaker) based on Class F design
Intrinsic Waveforms of Main and Peaker Amplifiers

Main PA Waveforms at Full Power

Peaker PA Waveforms at Full Power

Main PA Waveforms at 7.5 dB OBO

Peaker PA Waveforms at 7.5 dB OBO

Copyright © 2013, Cree, Inc.
The effect of active load pull from the peaker PA on the intrinsic drain waveforms of the main PA

To the authors’ knowledge this is the first published example of such a time domain simulation

The effect of active load pull from the peaker PA on the intrinsic dynamic load-lines of the main PA
**Conclusions**

- Cree Large-Signal Models for GaN HEMT transistors have been extended to include 6 port functionality
  - Drain, Gate, Source
  - Intrinsic Drain Current
  - Intrinsic Drain Voltage
  - Temperature Sense
- Additional “intrinsic” ports allow easy and accurate inspection of “true” drain voltages and current waveforms
  - Useful for waveform-engineered amplifiers
  - Useful for “continuous” Class E and F simulations allowing maintenance of high efficiency and acceptable linearity over wide bandwidths
  - Additional design ability to check for PA ruggedness
  - Allows waveform engineering for 2 and N-way Doherty PA’s